20” TFT TV

SERVICE MANUAL
(17MB18)

TABLE OF CONTENTS

1. INTRODUCTION

1.1. Scope

The document covers 20” (17MB18) chassis building blocks, basic features, service menu settings, and the other information needed by service personal.

1.2. General Features

The system is a 14” to 20” TFT LCD TV solution with UOCIII Versatile Signal Processor and PW1306 Video Image Processor chip-set on 4-layer PCB. The TV will support PAL/SECAM B/G/D/K/I/L/L’.
The other general default features of the TV are as listed below:

- 1 Full Scart input (with SVHS support)
- 1 SVHS input through standard S-Video interface.
- 1 CVBS input through standard RCA jack
- 75 ohms antenna input
- D-Sub 15 PC Input
- GERMAN + NICAM STEREO
- <**3**W S/B Power Consumption from mains supply
- 2x3W Speaker Output Power @16 Ohm spks; HP Output, Stereo Audio line out
- Stereo Audio line in
- Equalizer
- IR Control (RC5)
- OSD;Menu Languages ENG, FRA, GER, ITA, SPA, POR, TUR, SWE, DEN, FIN, NOR, POL, HUN, CZE, BUL, ARA, PER, RUS (subject to change and be grouped)
- Teletext
- 2H/4H Comb Filter
- White balance settings (warm/normal/cool) for TV&PC
- Full AIR&CABLE band coverage
- Auto Shut down

2. SYSTEM BUILDING BLOCKS

17MB18 chassis main blocks are as follows:

- **Analog Front End** : UOCIII (Microcontroller + Video Proccessor + Sound Proccessor + IF), CTI, Tuner, SAW filters, Audio Amp., DAC
- **Back End** : PW1306(Microcontroller, Scaler, OSD, Keyboard/IR Interface)
- **Side Board(s)** : Keyboards, IR/LED Boards, TTL Panel Interface Cards, VCbCr Input Board (Optional)

2.1. Analog Front End

17MB18 Main Board consists of two major blocks. The first block is analog front-end and this block is handled by UOCIII chip that is highly multifunctional. This IC does demodulation of Video & Audio from Tuner IF, CVBS, Audio, RGB, SVHS input selection and processing. It has an audio processor that supports equalizer or tone control, volume control, AVL, surround effect etc and supplies amplifier, headphone and CVBS & audio line outputs. It handles video processing such as colour standard detection and demodulation, picture alignment (brightness, contrast, colour etc.). The IC also does teletext decoding with 10 pages text memory. After video processing, the processed video is applied to PW1306 chip in RGB format.

The TV Tuner is an asymmetrical IF output type and is PLL controlled. For multistandard reception, a switchable SAW filter is used as the sound filter and it is controlled by SAW_SW output from UOC. After the SAW filter block, IF signal is applied to UOC IF inputs (VIFIN[1,2] and SIF[1,2]).

As UOCIII can handle all the audio processing, there is no need for additional audio processor solution on the board. UOC supports three Audio outputs. These outputs are assigned to Headphone, Speaker and Scart Audio line outputs. The board employs TDA7056A and TDA1308 to drive speaker and headphone outputs respectively. As another dedicated output for Audio Line out from jack is not possible in UOC, this line out signal is obtained by using I2S input DAC CS4335. UOCIII I2S output is converted to anolog signal by DAC CS4335.

2.1.1. Tuner

As the thickness of the TV set has a limit, a horizontal mounted tuner with longer connector is used in the product. The tuning is available through the digitally controlled I^2C bus (PLL). Below you will find info on the Asymmetrical Tuner in use.

General description:

The tuner meets a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance drives a wide variety of SAW filters with sufficient suppression of triple transient.

Features:

- Small sized UHF/VHF tuners
- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally controlled (PLL) tuning via I^2C-bus
- Off-air channels, S-cable channels and Hyper band
- $Z_{S(AE)}$ Aerial source impedance (unbalanced) 75 Ohm

PIN	SYMBOL	DESCRIPTION
1	AGC	Automatic Gain Control Voltage 4 ±0.1
2	TU	Tuning voltage monitor (output)
3	AS	I 2C-Bus Address Select
4	SCL	I 2C-Bus Serial Clock
5	SDA	I 2C-Bus Serial Data
6	n.c.	Not Connected
7	V_S	Supply Voltage +5V ±0.125
8	ADC	ADC Input
9	V_{ST}	Fixed tuning Supply Voltage +33V ±0.5

10	I.F out 2	Symmetrical I.F output 2 / Do not connect for asymmetrical
11	I.F out 1	Asymmetrical I.F Output / Symmetrical I.F output 1
M1,M2,M3, M4	GND	Mounting Tags (Ground)

2.1.2. SAW Filters

K3953M is an IF Filter for Video Applications. The package is SIP5K. Supported standards are B/G, D/K, I, L/L'.
K9656M is an IF Filter for Audio Applications. The package is SIP5K. Supported standards are B/G, D/K, I, L/L'.

2.2. Back End

The Back End section is handled by PW1306 chip. This IC has built in ADC's for RGB and SOY support. The RGB input can handle standard interlaced RGB output from UOC, PC VGA RGB input. As only 1 set of ADC is present in PW1306 these sources should be multiplexed.
All the multiplexing operations are controlled by PW1306 via YUV_TV_SW (58) and VGA_TV_SW (57) signals.

A: VGA _TV_SW B: YUV _TV_SW		
A	**B**	**SYNC SOURCE**
0	0	UOC
0	1	VGA
1	0	YcbCr
1	1	NOT USED

Table 2: H/V Sync Multiplexing Table

The video output from PW1306 is a 48-bit digital RGB bus format and made available on two separate connectors with TTL control signals (i.e. HS, VS, CLK, etc.). This digital output is intended to interface to TTL compatible display devices. As PW1306 does not have integrated LVDS transmitter, 24 bit (even part of RGB) video output and TTL control signals from PW1306 are also inputted to DS90C385 LVDS IC to produce single pixel LVDS output for LVDS compatible LCDs.

Backlight control is also possible via PW1306 Porta7 pin (PWMOUT, PL176-10), that is a variable duty-cycle pulse generator output.

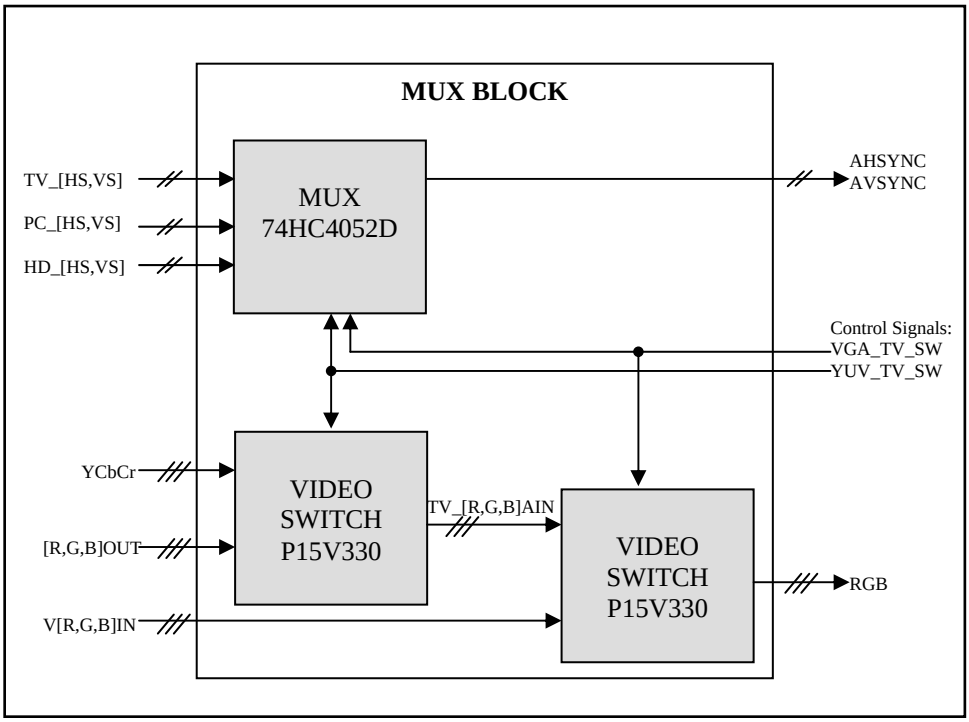


Figure 1: MUX Block.

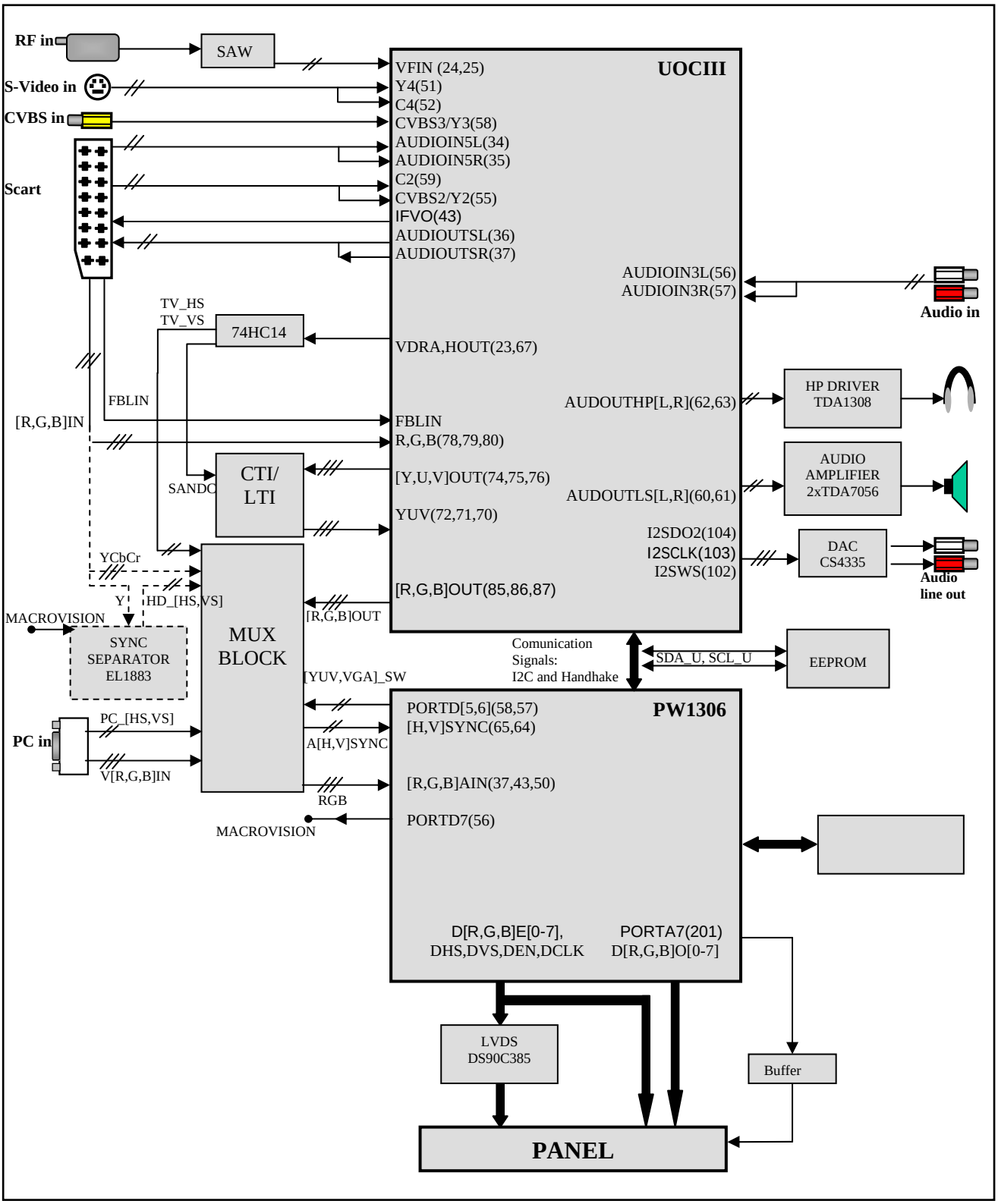


Figure 2: TV system block diagram.

2.3. Side Board(s)

2.3.1. Keypads

The keypads (17TK15, 16, 17, 20, 21) for 17MB18 main board are listed in the Table below. (They have the same connector pinning though):

			17"
Key Name	Type	Function	21
Power	Soft sw.	Power shut-down and turn on	X
Stand-by	Tact sw.	Switch between stand-by and turn on modes.	-
TV/AV	Tact sw.	Input source select button.	X
Menu	Tact sw.	Display main menu on the screen. If any menu is active, display the upper menu. If main menu is active, turn menu off.	X
Program-	Tact sw.	Go to the lower program at any time in TV mode. In menu mode, go to down menu item.	X
Program+	Tact sw.	Go to the upper program at any time in TV mode. In menu mode, go to up menu item.	X
Volume-	Tact sw.	Decrease the volume level in the volume. In menu mode, go to left menu item.	X
Volume+	Tact sw.	Increase the volume level in the volume. In menu mode, go to right menu item.	X

Connector PL1 on keypads (connected to the connector PL175 on the main board):

Pin No:	Name	Pin No:	Name:
1	Volume+	6	Program+
2	Volume-	7	Program-
3	Ground	8	Menu
4	Not Connected*	9	TV/AV
5	Ground	10	Stand-by/Shut-down

*Reserved: It can be +5V in the future designs if needed.

2.3.2. IR&Led Board

IR&LED board contains LED indicator(s) to show TV's status (Red for stand-by, green for normal operation) and one IR receiver to get remote control instructions. All the IR&LED boards have the same circuit and connector pinning but the different mechanical structure to fit different cabinets (see the related section for schematics and connector pinning).

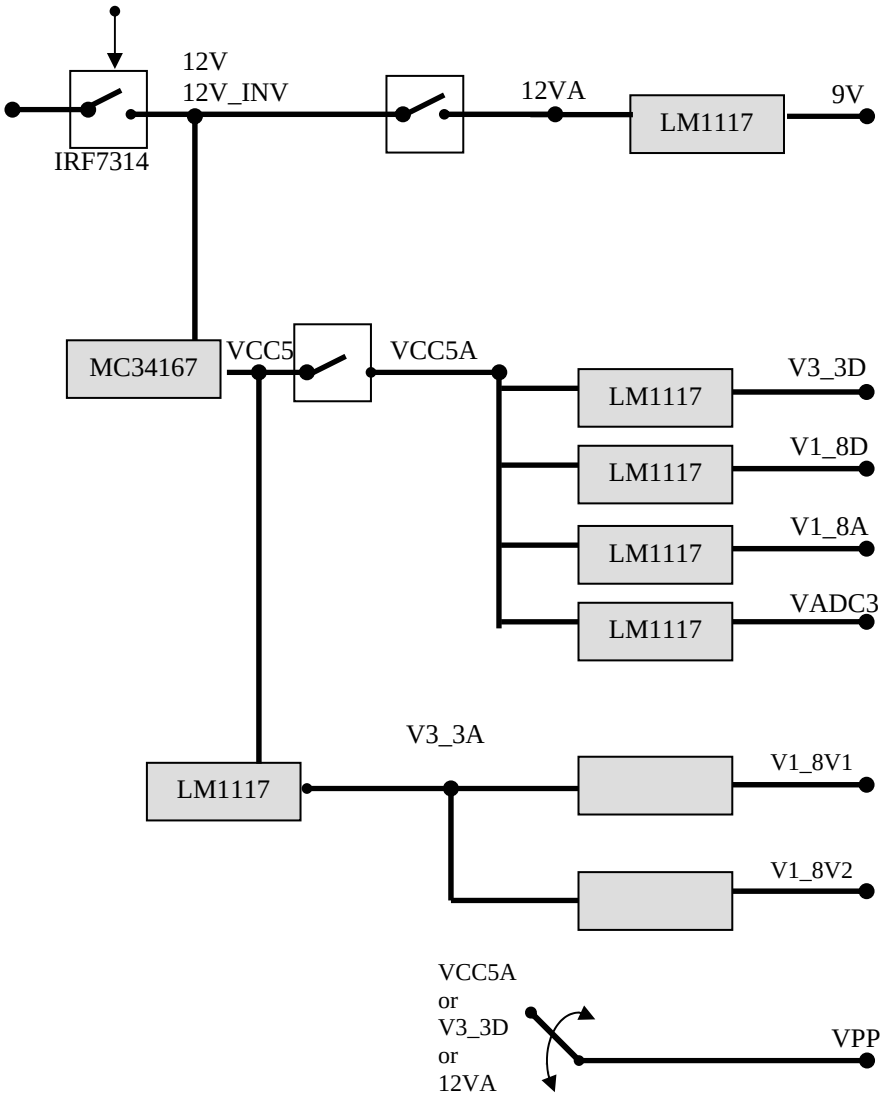
2.4. Power

Several linear regulators and switches are used to generate several separate analog and digital voltage supplies such as +5, +3.3, +1.8, etc. (Please check the Figure 3, and Table 3 for power management details.)

SIGNAL	SUPPLIED ICs	OFF AT STDBY	ALWAYS ON	SUPPLY
12V_INV	Panel Inverter	-	-	PSU
12VA	IC410, IC411 Audio Amplifiers	X		PSU

SIGNAL	SUPPLIED ICs	OFF AT STDBY	ALWAYS ON	SUPPLY
9V	IC200 TA1366FG	X		LM1117
VCC5A	IC203 UOC, TU200 Tuner, Sync Circuit, IC401 Headphones, IC402 MUX Block, IC400 DDC-EEPROM	X		IC505, MC3416
V3_3A	IC203 UOC, IC175 Keypad I/O, IC101 I2C-EEPROM		X	IC502, LM1117
V3_3D	IC100 PW1306, IC102 Flash, IC176 LVDS, ,	X		IC500, LM1117
V1_8D	IC100 PW1306	X		IC501, LM1117
V1_8A	IC100 PW1306	X		IC504, LM1117
VADC3	IC100 PW1306	X		IC503, LM1117
V1_8V1	IC203 UOC		X	
V1_8V2	IC203 UOC		X	
VPP	Panel Display Electronics	X		

Table 3: Power management table.


12V
12V_INV
12VA
9V
LM1117
IRF7314
MC34167
VCC5
VCC5A
V3_3D
LM1117
V1_8D
LM1117
V1_8A
LM1117
VADC3
LM1117
V3_3A
LM1117
V1_8V1
V1_8V2
VCC5A
or
V3_3D
or
12VA
VPP

3. IC AND COMPONENT DESCRIPTIONS

3.1. Basic IC List

No	Title	Description
IC203	UOCIII	Versatile Signal Processor
IC100	PW1306	Video Image Processor with Analog Interface
IC102	MT28F800B3W	Flash Memory
IC176	DS90C385	Programmable LVDS Transmitter
IC103	EL1883	Sync Separator
IC405, IC402	P15V330	Wide Bandwidth 2-channel Multiplexer/Demultiplexer
IC404	74HC4052	Dual 4-channel Analog Multiplexer
IC200	TA1366FG	LTI/CTI IC
IC410, IC411	TDA7056A	Class AB Mono 3W Power Amplifier
IC401	TDA1308	Class AB Stereo Headphone Driver
IC500/1/2/3/4, IC201	LM1117	Linear Regulator
IC400	24LC21	
IC101	24LC32	Serial Electrically Erasable PROM

3.2. UOCIII

The UOCIII series combines the functions of a Video Signal Processor (VSP) together with a FLASH embedded TEXT/Control/Graphics m-Controller (TCG m-Controller) and US Closed Caption decoder. In addition the following functions can be added:

- Adaptive digital (4H/2H) PAL/NTSC combfilter
- Teletext decoder with 10 page text memory
- Multi-standard stereo decoder
- BTSC stereo decoder
- Digital sound processing circuit
- Digital video processing circuit

The UOC III series consists of the following 3 basic concepts:

- Stereo versions. These versions contain the TV processor with a stereo audio selector, the TCG m-Controller, the multi-standard stereo or BTSC decoder, the digital sound processing circuit and the digital video processing circuit. Options are the adaptive digital PAL/NTSC comb filter and a teletext decoder with 10 page text memory.
- AV stereo versions. These versions contain the TV processor with stereo audio selector and the TCG m-Controller. Options are the digital sound processing circuit, the digital video processing circuit, the adaptive digital PAL/NTSC comb filter and a teletext decoder with a 10 page text memory.
- Mono sound versions. These versions contain the TV processor with a selector for mono audio signals and the TCG m-Controller. Options are the adaptive digital PAL/NTSC combfilter and a teletext decoder with 10 page text memory.

3.2.1. Pinout

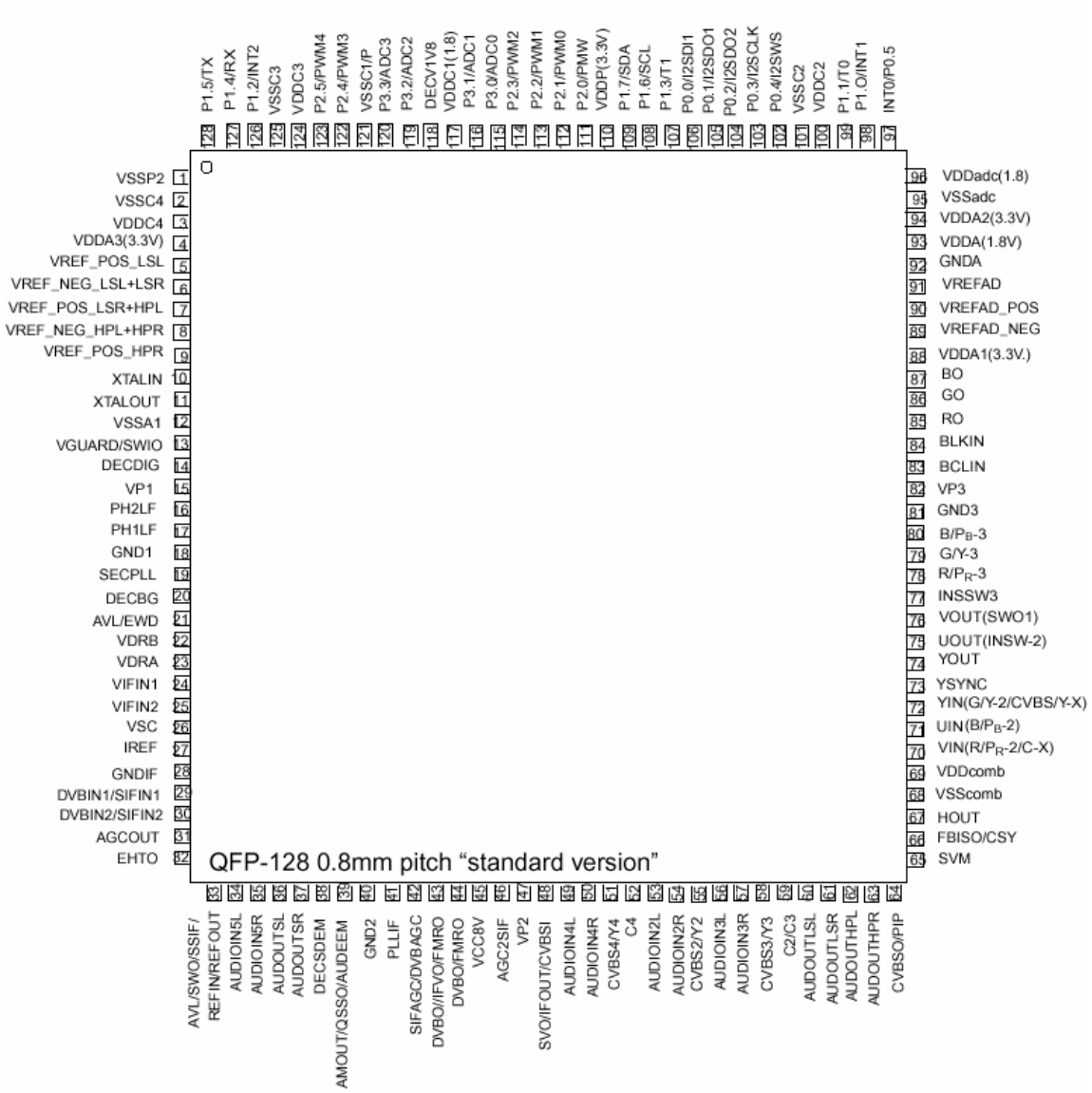


Figure 6: UOCIII Pin configuration “stereo” and “AV-stereo” versions with Audio DSP

SYMBOL	STEREO +AV STEREO	AV STEREO NO AUDIO DSP	MONO	DESCRIPTION
VSSP2	1	1	1	ground
VSSC4	2	2	2	ground
VDDC4	3	3	3	digital supply to SDACs (1.8V)
VDDA3(3.3V)	4	4	4	supply (3.3 V)
VREF_POS_LSL	5	-	-	positive reference voltage SDAC (3.3 V)
VREF_NEG_LSL+HPL	6	-	-	negative reference voltage SDAC (0 V)
VREF_POS_LSR+HPR	7	-	-	positive reference voltage SDAC (3.3 V)

SYMBOL	STEREO +AV STEREO	AV STEREO NO AUDIO DSP	MONO	DESCRIPTION
VREF_NEG_HPL+HPR	8	-	-	negative reference voltage SDAC (0 V)
VREF_POS_HPR	9	-	-	positive reference voltage SDAC (3.3 V)
XTALIN	10	10	10	crystal oscillator input
XTALOUT	11	11	11	crystal oscillator output
VSSA1	12	12	12	ground
VGUARD/SWIO	13	13	13	V-guard input / I/O switch (e.g. 4 mA current sinking capability for direct drive of LEDs)
DECDIG	14	14	14	decoupling digital supply
VP1	15	15	15	1st supply voltage TV-processor (+5 V)
PH2LF	16	16	16	phase-2 filter
PH1LF	17	17	17	phase-1 filter
GND1	18	18	18	ground 1 for TV-processor
SECPLL	19	19	19	SECAM PLL decoupling
DECBG	20	20	20	bandgap decoupling
EWD/AVL (1)	21	21	21	East-West drive output or AVL capacitor
VDRB	22	22	22	vertical drive B output
VDRA	23	23	23	vertical drive A output
VIFIN1	24	24	24	IF input 1
VIFIN2	25	25	25	IF input 2
VSC	26	26	26	vertical sawtooth capacitor
IREF	27	27	27	reference current input
GNDIF	28	28	28	ground connection for IF amplifier
SIFIN1/DVBIN1 (2)	29	29	29	SIF input 1 / DVB input 1
SIFIN2/DVBIN2 (2)	30	30	30	SIF input 2 / DVB input 2
AGCOUT	31	31	31	tuner AGC output
EHTO	32	32	32	EHT/overvoltage protection input
AVL/SWO/SSIF/ REFO/REFIN (2)(3)	33	33	33	Automatic Volume Levelling / switch output / sound IF input / subcarrier reference output / external reference signal input for I signal mixer for DVB operation
AUDIOIN5	-	-	34	audio 5 input
AUDIOIN5L	34	34	-	audio-5 input (left signal)
AUDIOIN5R	35	35	-	audio-5 input (right signal)
AUDOUTSL	36	36	-	audio output for SCART/CINCH (left signal)
AUDOUTSR	37	37	-	audio output for SCART/CINCH (right signal)
DECSDEM	38	38	38	decoupling sound demodulator
QSSO/AMOUT/AUDEEM (2)	39	39	39	QSS intercarrier output / AM output / deemphasis (front-end audio out)
GND2	40	40	40	ground 2 for TV processor
PLLIF	41	41	41	IF-PLL loop filter

SYMBOL	STEREO +AV STEREO	AV STEREO NO AUDIO DSP	MONO	DESCRIPTION
SIFAGC/DVBAGC (2)	42	42	42	AGC sound IF / internal-external AGC for DVB applications
DVBO/IFVO/FMRO (2)	43	43	43	Digital Video Broadcast output / IF video output / FM radio output
DVBO/FMRO (2)	44	44	-	Digital Video Broadcast output / FM radio output
VCC8V	45	45	45	8 Volt supply for audio switches
AGC2SIF	46	-	-	AGC capacitor second sound IF
VP2	47	47	47	2ndsupply voltage TV processor (+5 V)
IFVO/SVO/CVBSI (2)	48	48	48	IF video output / selected CVBS output / CVBS input
AUDIOIN4	-	-	49	audio 4 input
AUDIOIN4L	49	49	-	audio-4 input (left signal)
AUDIOIN4R	50	50	-	audio-4 input (right signal)
CVBS4/Y4	51	51	51	CVBS4/Y4 input
C4	52	52	52	chroma-4 input
AUDIOIN2	-	-	53	audio 2 input
AUDIOIN2L/SSIF (3)	53	53	-	audio 2 input (left signal) / sound IF input
AUDIOIN2R	54	54	-	audio 2 input (right signal)
CVBS2/Y2	55	55	55	CVBS2/Y2 input
AUDIOIN3	-	-	56	audio 3 input
AUDIOIN3L	56	56	-	audio 3 input (left signal)
AUDIOIN3R	57	57	-	audio 3 input (right signal)
CVBS3/Y3	58	58	58	CVBS3/Y3 input
C2/C3	59	59	59	chroma-2/3 input
AUDOUTLSL	60	62	-	audio output for audio power amplifier (left signal)
AUDOUTLSR	61	63	-	audio output for audio power amplifier (right signal)
AUDOUT/AMOUT/FMOUT	-	-	62	audio output / AM output / FM output, volume controlled
AUDOUTHPL	62	-	-	audio output for headphone channel (left signal)
AUDOUTHPR	63	-	-	audio output for headphone channel (right signal)
CVBSO/PIP	64	64	64	CVBS / PIP output
SVM	65	65	65	scan velocity modulation output
FBISO/CSY	66	66	66	flyback input/sandcastle output or composite H/V timing output
HOUT	67	67	67	horizontal output
VSScomb	68	68	68	ground connection for comb filter
VDDcomb	69	69	69	supply voltage for comb filter (5 V)
VIN (R/PRIN2/CX)	70	70	70	V-input for YUV interface (2ndR input / PRinput or Cxinput)
UIN (B/PBIN2)	71	71	71	U-input for YUV interface (2ndB input / PB input)
YIN (G/YIN2/CVBS-YX)	72	72	72	Y-input for YUV interface (2nd G input / Y input or CVBS/Yxinput))
YSYNC	73	73	73	Y-input for sync separator

SYMBOL	STEREO +AV STEREO	AV STEREO NO AUDIO DSP	MONO	DESCRIPTION
YOUT	74	74	74	Y-output (for YUV interface)
UOUT (INSSW2)	75	75	75	U-output for YUV interface (2ndRGB / YP_BP_R insertion input)
VOUT (SWO1)	76	76	76	V-output for YUV interface (general purpose switch output)
INSSW3	77	77	77	3rdRGB / YP_BP_R insertion input
R/P_RIN3	78	78	78	3rdR input / $P_R$input
G/YIN3	79	79	79	3rdG input / Y input
B/P_BIN3	80	80	80	3rdB input / $P_B$input
GND3	81	81	81	ground 3 for TV-processor
VP3	82	82	82	3rdsupply for TV processor
BCLIN	83	83	83	beam current limiter input
BLKIN	84	84	84	black current input
RO	85	85	85	Red output
GO	86	86	86	Green output
BO	87	87	87	Blue output
VDDA1	88	88	88	analog supply for TCG m-Controller and digital supply for TV-processor (+3.3 V)
VREFAD_NEG	89	89	89	negative reference voltage (0 V)
VREFAD_POS	90	90	90	positive reference voltage (3.3 V)
VREFAD	91	-	-	reference voltage for audio ADCs (3.3/2 V)
GNDA	92	92	92	ground
VDDA(1.8V)	93	93	93	analogue supply for audio ADCs (1.8 V)
VDDA2(3.3)	94	94	94	supply voltage SDAC (3.3 V)
VSSadc	95	95	95	ground for video ADC and PLL
VDDadc(1.8)	96	96	96	supply voltage video ADC and PLL
INT0/P0.5	97	97	97	external interrupt 0 or port 0.5 (4 mA current sinking capability for direct drive of LEDs)
P1.0/INT1	98	98	98	port 1.0 or external interrupt 1
P1.1/T0	99	99	99	port 1.1 or Counter/Timer 0 input
VDDC2	100	100	100	digital supply to core (1.8 V)
VSSC2	101	101	101	ground
P0.4/I2SWS	102	-	-	port 0.4 or I^2S word select
P0.4	-	102	102	port 0.4
P0.3/I2SCLK	103	-	-	port 0.3 or I^2S clock
P0.3	-	103	103	port 0.3
P0.2/I2SDO2	104	-	-	port 0.2 or I^2S digital output 2
P0.2	-	104	104	port 0.2
P0.1/I2SDO1	105	-	-	port 0.1 or I^2S digital output 1
P0.1	-	105	105	port 0.1

SYMBOL	STEREO +AV STEREO	AV STEREO NO AUDIO DSP	MONO	DESCRIPTION
P0.0/I2SDI1/O	106	-	-	port 0.0 or I2S digital input 1 or I2S digital output
P0.0	-	106	106	port 0.0
P1.3/T1	107	107	107	port 1.3 or Counter/Timer 1 input
P1.6/SCL	108	108	108	port 1.6 or I2C-bus clock line
P1.7/SDA	109	109	109	port 1.7 or I2C-bus data line
VDDP(3.3V)	110	110	110	supply to periphery and on-chip voltage regulator (3.3 V)
P2.0/TPWM	111	111	111	port 2.0 or Tuning PWM output
P2.1/PWM0	112	112	112	port 2.1 or PWM0 output
P2.2/PWM1	113	113	113	port 2.2 or PWM1 output
P2.3/PWM2	114	114	114	port 2.3 or PWM2 output
P3.0/ADC0	115	115	115	port 3.0 or ADC0 input
P3.1/ADC1	116	116	116	port 3.1 or ADC1 input
VDDC1	117	117	117	digital supply to core (+1.8 V)
DECV1V8	118	118	118	decoupling 1.8 V supply
P3.2/ADC2	119	119	119	port 3.2 or ADC2 input
P3.3/ADC3	120	120	120	port 3.3 or ADC3 input
VSSC/P	121	121	121	digital ground for m-Controller core and periphery
P2.4/PWM3	122	122	122	port 2.4 or PWM3 output
P2.5/PWM4	123	123	123	port 2.5 or PWM4 output
VDDC3	124	124	124	digital supply to core (1.8V)
VSSC3	125	125	125	ground
P1.2/INT2	126	126	126	port 1.2 or external interrupt 2
P1.4/RX	127	127	127	port 1.4 or UART bus
P1.5/TX	128	128	128	port 1.5 or UART bus

3.3. PW1306

The PW1306 Video Image Processor is a “system-on-a-chip ” that oversamples and processes RGB or YPbPr video from analog video decoders. The PW1306 integrates video processing, including deinterlacer and video enhancement filters with a triple ADC. Analog RGB or YPbPr in PC graphics, standard, or high-definition video can be displayed in either 4:3 or 16:9 formats.

- Supports analog video decoders with triple 8-bit Analog-to-Digital Converters (ADCs) up to 140 MSPS conversion rate
- Supports Sync-on-Green (SOG), Sync-on-Luma (SOY),and Composite sync inputs
- 1080i/720p/480p HDTV; 480i and 576i NTSC/PAL SDTV; PC graphics (up to SXGA)
- YPbPr/YCbCr/YUV-to-RGB Color Space Converter with programmable coefficients
- On-chip, bitmap-based, OSD controller with on-chip memory
- 24/30/48-bit RGB output with 135 MPixels/second maximum output rate

3.3.1. Pinout

This section lists the pin functions for the PW1306 208-pin PQFP package. Pin types include:

- I/O SR5 (I/O slew rate-controlled,5V input tolerant)

- I/O D5 (bidirectional, 5-volt tolerant with pull-down)
- I/O U5 (bidirectional, 5-volt tolerant with pull-up)
- ID 5 (input, 5-volt tolerant with pull-down)
- OS (output with fixed slew-rate control)
- AI (analog input, 5-volt tolerant)
- DI (digital input, 5-volt tolerant)
- DIS (digital input, 5-volt tolerant, Schmitt trigger)
- I (XTALIN)
- (XTALOUT)
- P (power)
- NC (no connect)
- BOD (bidirectional open drain)
- OSR (output with slew rate)

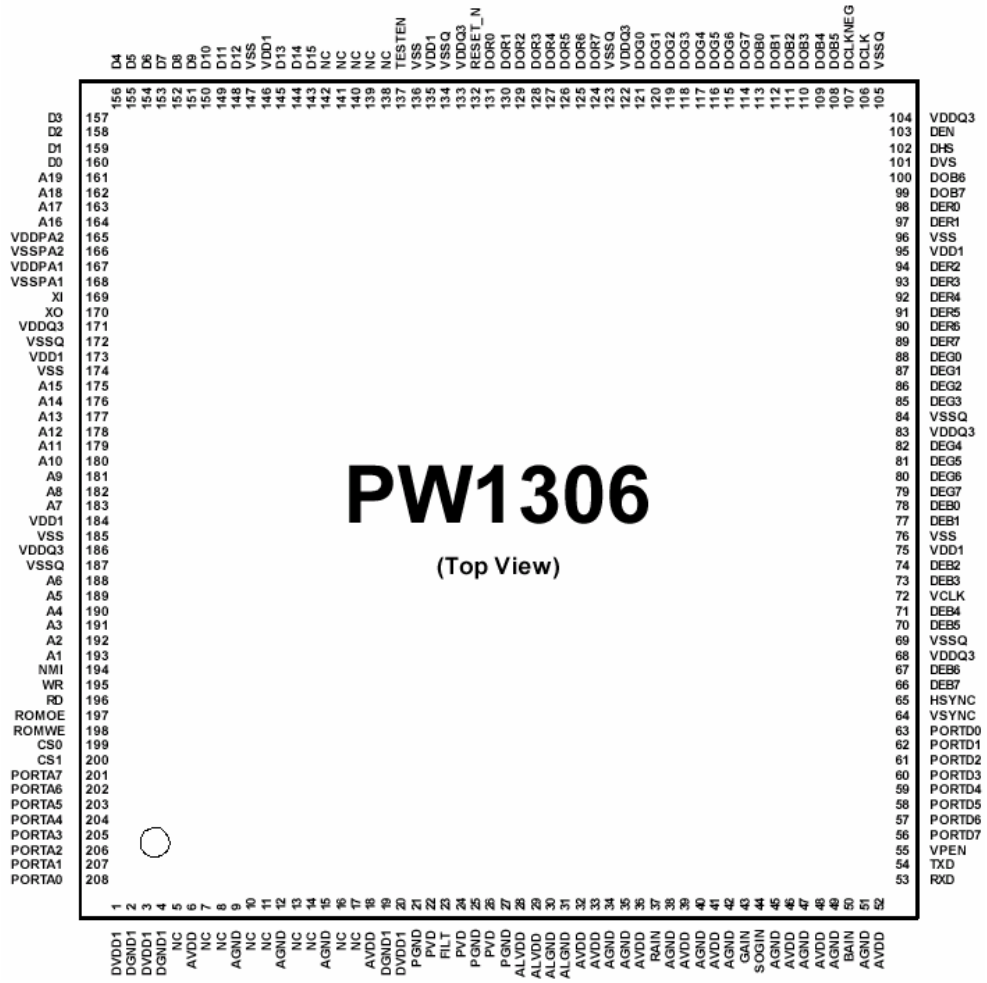


Figure 8: PW1306 Pin configuration.

Signal	Pin	Type	Function
RAIN	37	AI	Red/Green/Blue Analog Inputs. These pins receive the Red, Green and Blue, or YPbPr/YCbCr/YUV analog signals from the analog video source. For proper operation of the clamp feature, these inputs must be AC-coupled.
GAIN	43	AI	
BAIN	50	AI	

Signal	Pin	Type	Function
SOGIN	44	AI	Analog Sync-On-Green or Sync-On-Luma input. Allows recovery of the HSYNC signal when this pin is AC-coupling to the Green (Red or Blue) analog signal source. If not used, this pin should be left unconnected.
FILT	23	AI	External PLL Loop Filter. When using the on-chip PLL, this pin must be connected to an external filter network.
HSYNC	65	DIS	Horizontal Synchronization Input. This digital input signal controls the horizontal scan frequency by synchronizing the start of the horizontal scan. The logic polarity of this signal is controlled by the HSPOL bit.
VSYNC	64	DIS	Vertical Synchronization Input. This digital signal controls the vertical scan frequency.
DCLK	106	OSR	DPort Pixel Clock. Output clock for the display port pixel data. DCLK is enabled by the DCLKEN bit and can be inverted by the DCPOL bit. DCLK can be set to run at ½ pixel rate, for dual pixel output mode, by setting the DCK2EN bit. The internal DCLK clock domain can be disabled by the DCLKOFF bit to reduce power consumption.
DCLKNEG	107	OSR	DPort Pixel Clock.
DVS	101	OS	DPort Vertical Sync. DVS can be either active-high or active-low depending on the VSPOL bit. Width and timing is controlled by the VPLSE and VDLY registers.
DHS	102	OS	DPort Vertical Sync. DHS can be either active-high or active-low depending on the HSPOL bit. Sync width can be controlled by the HPLSE register.
DEN	103	OS	DPort Pixel Enable. This signal is active whenever valid data is present. The polarity is specified by the DENPOL bit.
DER0	98	OSR	DEPort Red Pixel Data. In dual pixel output mode these pins are the EVEN red outputs.
DER1	97	OSR	
DER2	94	OSR	
DER3	93	OSR	
DER4	92	OSR	
DER5	91	OSR	
DER6	90	OSR	
DER7	89	OSR	

Signal	Pin	Type	Function
DEG0	88	OSR	DEPort Green Pixel Data. In dual pixel output mode these pins are the EVEN green outputs.
DEG1	87	OSR	
DEG2	86	OSR	
DEG3	85	OSR	
DEG4	82	OSR	
DEG5	81	OSR	
DEG6	80	OSR	
DEG7	79	OSR	
DEB0	78	OSR	DEPort Blue Pixel Data. In dual pixel output mode these pins are the EVEN blue outputs.
DEB1	77	OSR	
DEB2	74	OSR	
DEB3	73	OSR	
DEB4	71	OSR	
DEB5	70	OSR	
DEB6	67	OSR	
DEB7	66	OSR	
VCLK	72	I/O D5	DVPort Pixel Clock. The VCLK pin is used for DV port image capture. The polarity can be selected by the VCLKPOL bit.
VPEN	55	I/O D5	DVPort Pixel Enable. Used when external flow control capture mode is enabled by the EXTFCE bit. When VPEN is active, the input data is valid. The polarity can be selected by the PENPOL bit. Use of this pin allows non-contiguous input data.

Signal	Pin	Type	Function
PORTD[0-7]	[56-63]	I/O	PORTD(7:0) can be used as GPO (Output Only).
DOR0	131	I/O SR5	DOPort Red Pixel Data. In dual pixel output mode these pins are the ODD red outputs. In single pixel output mode these pins are not used.
DOR1	130	I/O SR5	
DOR2	129	I/O SR5	
DOR3	128	I/O SR5	
DOR4	127	I/O SR5	
DOR5	126	I/O SR5	
DOR6	125	I/O SR5	
DOR7	124	I/O SR5	
DOG0	121	I/O SR5	DOPort Green Pixel Data. In dual pixel output mode these pins are the ODD green outputs. In single pixel output mode these pins are not used.
DOG1	120	I/O SR5	
DOG2	119	I/O SR5	
DOG3	118	I/O SR5	
DOG4	117	I/O SR5	
DOG5	116	I/O SR5	
DOG6	115	I/O SR5	
DOG7	114	I/O SR5	
DOB0	113	I/O SR5	DOPort Blue Pixel Data. In dual pixel output mode these pins are the ODD blue outputs. In single pixel output mode these pins are not used.
DOB1	112	I/O SR5	

Signal	Pin	Type	Function
DOB2	111	I/O SR5	
DOB3	110	I/O SR5	
DOB4	109	I/O SR5	
DOB5	108	I/O SR5	
DOB6	100	I/O SR5	
DOB7	99	I/O SR5	
WR	195	I/O D5	Write Enable. Low indicates a write to external RAM or other devices.
RD	196	I/O D5	Read Enable. Low indicates a read to external RAM or other devices.
ROMOE	197	OS	ROM Output Enable. Low output indicates a read from external ROM.
ROMWE	198	OS	ROM Write Enable. Low indicates a write to external ROM.
CS0	199	I/O D5	Miscellaneous Chip Select 0. Low selects external devices.
CS1	200	I/O D5	Miscellaneous Chip Select 1. When EXTRAMEN=0, low selects external devices. Chip select for external RAM. When EXTRAMEN=1, low selects external RAM. (RAMCS)
NMI	194	ID 5	Non-Maskable Interrupt. A high input triggers a non-maskable interrupt to the on-chip microprocessor.
A1	193	I/O D5	Microprocessor address bus output bits (19:1).
A2	192	I/O D5	
A3	191	I/O D5	
A4	190	I/O D5	
A5	189	I/O D5	
A6	188	I/O D5	
A7	183	I/O D5	
A8	182	I/O D5	
A9	181	I/O D5	
A10	180	I/O D5	
A11	179	I/O D5	

Signal	Pin	Type	Function
A12	178	I/O D5	
A13	177	I/O D5	
A14	176	I/O D5	
A15	175	I/O D5	
A16	164	I/O D5	
A17	163	I/O D5	
A18	162	I/O D5	
A19	161	I/O D5	
D0	160	I/O D5	Microprocessor 16-bit bidirectional data bus.
D1	159	I/O D5	
D2	158	I/O D5	
D3	157	I/O D5	
D4	156	I/O D5	
D5	155	I/O D5	
D6	154	I/O D5	
D7	153	I/O D5	
D8	152	I/O D5	
D9	151	I/O D5	
D10	150	I/O D5	
D11	149	I/O D5	
D12	148	I/O D5	
D13	145	I/O D5	
D14	144	I/O D5	
D15	143	I/O D5	
PORTA0	208	I/O U5	General-purpose I/O port bit controlled by PADAT0 and PAEN0. This pin has one other possible function when EXTRAMEN=1. When EXTRAMEN=1 and PAEN0=0, PORTA1 is microprocessor address bit 0 (A0).

Signal	Pin	Type	Function
PORTA1	207	I/O U5	General-purpose I/O port bit controlled by PADAT1 and PAEN1. This pin has one other possible function when EXTRAMEN=1. When EXTRAMEN=1 and PAEN1=0, PORTA1 is microprocessor byte-high enable (BHEN)
PORTA2	206	I/O U5	General-purpose I/O port bit controlled by PADAT2 and PAEN2.
PORTA3	205	I/O U5	General-purpose I/O port bit controlled by PADAT3 and PAEN3. This pin can also function as an external clock source for DCLK (DCLKEXT) when both the internal PLLs are disabled or when DPLLBYP=1.
PORTA4	204	I/O U5	General-purpose I/O port bit controlled by PADAT4 and PAEN4. This pin has one other possible function when IREN=1. When IREN=1 and PAEN4=1, this pin can function as an input to the on-chip IR receiver 0. (IRRCVR0)
PORTA5	203	I/O U5	General-purpose I/O port bit controlled by PADAT5 and PAEN5. This pin has other possible functions depending on the IREN, EIEN registers. When EIEN=1 and PAEN5=1, this pin can function as an external interrupt to the on-chip CPU. When IREN=1 and PAEN5=1, this pin can function as an input to the on-chip IR receiver 1 (IRRCVR1). When DPLLBYP=1 and PAEN=0, this pin becomes the output of the DCLK PLL. This output can be routed through an external spread spectrum chip and then back into port A3 (DCLK input) to implement spread spectrum.
PORTA6	202	I/O U5	General-purpose I/O port bit controlled by PADAT6 and PAEN6. This pin has one other possible function when PREF1EN=1. When PREF1EN=1 and PAEN6=0, PORTA6 is a variable duty-cycle pulse reference generator (PWM) output controlled by PREF1HI and PREF1LO.
PORTA7	201	I/O D5	General-purpose I/O port bit controlled by PADAT7 and PAEN7. This pin has one other possible function when PREF0EN=1. When PREF0EN=1 and PAEN7=0, PORTA7 is a variable duty-cycle pulse reference generator (PWM) output controlled by PREF0HI and PREF0LO.
RXD	53	I/O U5	Serial Receive Data. RXD is the serial receive data for the on-chip serial port. This pin can also function as the 2-wire master data pin when 2WMEN=16.
TXD	54	I/O U5	Serial Transmit Data. TXD is the serial transmit data for the on-chip serial port. This pin can also function as the 2-wire master clock output pin when 2WMEN=16.
TESTEN	137	ID 5	Test Mode Enable. Connect to ground for normal operation.
RESET_N	132	BOD	Reset Output. RESET_N is a bidirectional pin that can be used to either drive external logic in the system or receive an external reset signal.
XI	169	I	Crystal Input. Connect to external crystal. XI can also function as the MCLK input LVTTL-level signal from an external oscillator.

Signal	Pin	Type	Function
XO	170	O	Crystal Output. Connect to external crystal.
VDD1	75, 95, 135, 146, 173, 184	P	1.8V digital core power.
VSS	76, 96, 136, 147, 174, 185	P	Digital core ground.
VDDQ3	68, 83, 104, 122, 133, 171, 186	P	3.3V digital I/O power.
VSSQ	69, 84, 105, 123, 134, 172, 187	P	Digital I/O ground.
VDDPA1	167	P	1.8V analog clock generator power.
VDDPA2	165	P	1.8V analog clock generator power.
VSSPA1	168	P	Clock generator analog ground.
VSSPA2	166	P	Clock generator analog ground.
PVD	22, 24, 26	P	1.8V PLL power.
PGND	21, 25, 27	P	PLL ground.
DVDD1	1, 3, 20	P	1.8V ADC digital power.
DGND1	2, 4, 19	P	ADC digital ground.
ALVDD	28, 29	P	1.8V ADC PLL power.
ALGND	30, 31	P	ADC PLL ground.
AVDD	6, 18, 32, 33, 36, 39, 41, 46, 48,	P	3.3V ADC analog power.

Signal	Pin	Type	Function
	52		
AGND	9, 12, 34, 35, 38, 40, 42, 45, 47, 49, 51	P	ADC analog ground.

3.4. M29W800AT

Low Voltage Single Supply Flash Memory to store PW1306 code.
ELECTRONIC SIGNATURE
– Manufacturer Code: 20h
– Top Device Code, M29W800AT: D7h

3.5. DS90C385

The DS90C385 transmitter converts 28 bits of LVCMOS/ LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec.

- 20 to 85 MHz shift clock support
- Tx power consumption <130 mW (typ) @85MHz Grayscale
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Up to 2.38 Gbps throughput
- Up to 297.5 Megabytes/sec bandwidth
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard

3.6. P15V330

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is for both RGB and composite video switching applications.

- 200 MHz bandwidth
- 3 Ohm on-resistance
- Switching at 10 ns
- 100 mA output current

3.7. 74HC4052

The 74HC/HCT4052 are dual 4-channel analog multiplexers/demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S0 and S1) and an active LOW enable input (E).

- Wide analog input voltage range: ± 5 V.
- Low “ON” resistance:

80 Ohm (typ.) at VCC - VEE = 4.5 V
70 Ohm (typ.) at VCC - VEE = 6.0 V
60 Ohm (typ.) at VCC - VEE = 9.0 V

3.8. TA1366FG

TA1366FG is an Analog Y Cb Cr picture signal improver in a 24-pin SSOP plastic package. TA1366FG functions are controlled via I2C bus.

- YCbCr 2inputs
- Through mode (Y bandwidth: 0dB@30MHz)
- Y block
- Sharpness
- SRT (LTI)
- Y Group Delay Correction (Shoot balance)
- Color Detail Enhancer (CDE) and Noise Detection
- Cb/Cr block
- Color SRT (CTI)
- Green Stretcher

3.9. TDA7056A

The TDA7056A is a mono BTL output amplifier with DCvolume control. It is designed for use in TV and monitors.

- Mute mode, No switch-on and off clicks,
- Thermal protection,
- Short-circuit proof,
- ESD protected on all pins.

3.10. TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package.

- Wide temperature range
- No switch on/off clicks
- Low power consumption
- Short-circuit resistant

PIN	SYMBOL	DESCRIPTION	PIN VALUE
1	OUTA	Output A (Voltage swing)	Min : 0.75V, Max : 4.25V
2	INA(neg)	Inverting input A	Vo(clip) : Min : 1400mVrms
3	INA(pos)	Non-inverting input A	2.5V
4	V_{SS}	Negative supply	0V
5	INB(pos)	Non-inverting input B	2.5V
6	INB(neg)	Inverting input B	Vo(clip) : Min : 1400mVrms
7	OUTB	Output B (Voltage swing)	Min : 0.75V, Max : 4.25V
8	V_{DD}	Positive supply	5V, Min : 3.0V, Max : 7.0V

3.11. LM1117

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. The output voltage is adjusted according to the formula shown in Figure 9.

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

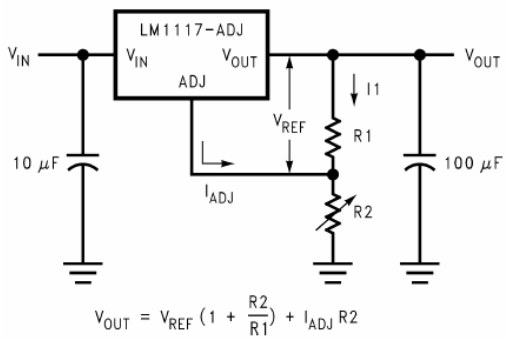
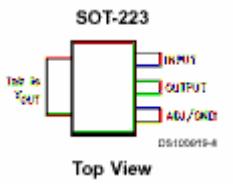
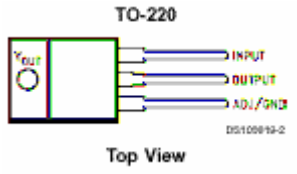
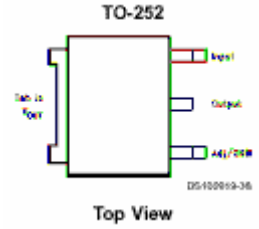


Figure 9: Basic adjustable regulator

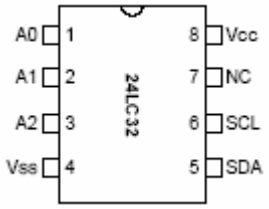






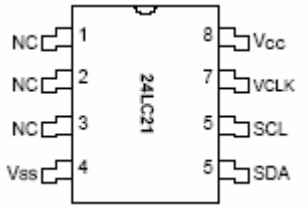
3.12. 24LC32

24LC32 is a 4K x 8 (32Kbit) Serial Electrically Erasable PROM capable of operation across a broad voltage range (2.5V to 6.0V).



3.13. 24LC21

24LC21 is a 128 x 8 bit Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information.



3.14. 74LVC541

The 74LVC541A is an octal non-inverting buffer/line driver with 5 V tolerant inputs/outputs. The 3-state outputs are controlled by the output enable inputs OE1and OE2.

- 5 V tolerant inputs/outputs; for interfacing with 5 V logic
- Wide supply voltage range from 2.7 to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels

INPUT			OUTPUT
OE1	OE2	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Pin no	Symbol	Name and function
1	OE1	Output Enable Input
2, 3, 4, 5, 6, 7, 8, 9	A0 to A7	Data Inputs
11, 12, 13, 14, 15, 16, 17, 18	Y0 to Y7	Data Outputs
	2A1 to 2A4	Data Inputs
	1Y1 to 1Y4	Data Outputs
19	OE2	Output Enable Input
10	GND	Ground (0V)
20	VCC	Positive Supply Voltage

3.15. SAA3010T

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section “Keyboard operation”.

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

Pin	Mnemonic	Function
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	sense mode selection input
3	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	Scan drivers
14	VSS	Ground (0V)
15-17	DR-2-DR0 (ODN)	Scan drivers
18	OSC (I)	Oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	Test point 1
21-27	X0-X6 (IPU)	Sense inputs from key matrix
28	VDD(I)	Voltage supply

Note:

(I): Input,
(IPU): input with p-channel pull-up transistor,
(ODN): output with open drain n-channel transistor
(OD3): output 3-state

3.16. MC34167

The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.
These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.
Protective features consist of cycle–by–cycle current limiting, under voltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 mA.

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Under voltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 mA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D 2 PAK Package
- Moisture Sensitivity Level (MSL) Equals 1

3.17. TFMS5360

The TFMS5360 is a miniature receiver for infrared remote control systems.

- Photo detector and preamplifier in one.
- 36 KHZ
- Pin diode and preamp
- IR filter.

3.18. Board Connectors, Headers & Jumpers

3.18.1. Analog PC Connector (PL400)

Pin #	Logic	I/O	Signal Description	Impedance
1	Analog	I	Red Component	75Ω
2	Analog	I	Green Comp.	75Ω
3	Analog	I	Blue Comp.	75Ω
13	TTL	I	Horizontal Sync	
14	TTL	I	Vertical Sync	
12	TTL	I/O	I2C Data	
15	TTL	I	I2C Clock	
9	Power	I	+5V	
5,6,7,8,10	Ground			
4,11	No Connect			

3.18.2. Scart Connector (PL401)

Pin	Signal	Description	Signal level	Impedance
1	SCOR1	Audio output (right)	0.5V rms	<1kohm
2	SCIR1	Audio input (right)	0.5V rms	>10kohm
3	SCOL1	Audio output (left)	0.5V rms	<1kohm
4		Ground (audio)	-	-
5		Ground	-	-
6	SCIL1	Audio input (left)	0.5V rms	>10kohm
7	BIN	Blue input	0.7V	75ohms
8	STATAV1	Function select (AV control)		>10kohm
9		Ground	-	-
10		Not connected	-	-
11	GIN	Green input	0.7V	75ohms
12		Not connected	-	-
13		Ground (red)	-	-
14		Ground (blanking)	-	-
15	RIN	Red input or Chrominance input	0.7V / 0.3V	75ohms
16	FBLIN	RGB switching control	High (1-3V) - RGB Low (0-0.4V) - Composite	75ohms
17		Ground (video input & output)	-	-
18		Ground (RGB switching control)	-	-
19	CVBSO2	Video output (composite)	1V including sync	75ohms
20	Y1SCART	Video input (composite) or Luminance input	1V including sync	75ohms
21		Common ground (shield)	-	-

3.18.3. S-Video Connector (JK403)

Pin	Signal	Impedance
1	Ground	
2	Ground	
3	Luminance	75Ω
4	Chrominance	75Ω

3.18.4. LVDS Panel Connector(1x20 PL179)

Pin	Symbol	Description
1	NC	
2	LVDS_GND	Ground
3	TXOUT3+	LVDS Signal(+)
4	TXOUT3-	LVDS Signal(-)
5	LVDS_GND	Ground
6	TXCLKOUT0+	LVDS Signal(+)
7	TXCLKOUT0-	LVDS Signal(-)
8	LVDS_GND	Ground
9	TXOUT2+	LVDS Signal(+)
10	TXOUT2-	LVDS Signal(-)
11	LVDS_GND	Ground
12	TXOUT1+	LVDS Signal(+)
13	TXOUT1-	LVDS Signal(-)
14	LVDS_GND	Ground
15	TXOUT0+	LVDS Signal(+)

Pin	Symbol	Description
16	TXOUT0-	LVDS Signal(-)
17	LVDS_GND	Ground
18	LVDS_GND	Ground
19	VPP	Power Supply (+5 or +3.3V)
20	VPP	Power Supply (+5 or +3.3V)

3.18.5. TTL Panel Connector -Even (2x17 PL177)

Pin	Symbol	Description	Pin	Symbol	Description
1	DBE6	Blue	18	DGE2	Green
2	DBE7	Blue	19	GND	Ground
3	DBE4	Blue	20	DGE0	Green
4	DBE5	Blue	21	DRE6	Red
5	GND	Ground	22	DRE7	Red
6	DBE3	Blue	23	DRE4	Red
7	DBE1	Blue	24	DRE5	Red
8	DBE2	Blue	25	GND	Ground
9	GND	Ground	26	DRE3	Red
10	DBE0	Blue	27	DRE1	Red
11	DGE6	Green	28	DRE2	Red
12	DGE7	Green	29	DEN	
13	DGE4	Green	30	DRE0	Red
14	DGE5	Green	31	DHS	
15	GND	Ground	32	DVS	
16	DGE3	Green	33	DCLK	
17	DGE1	Green	34	DCLK	

3.18.6. TTL Panel Connector -Odd (2x17 PL178)

Pin	Symbol	Description	Pin	Symbol	Description
1	DBO7	Blue	18	DGO1	Green
2	DBO6	Blue	19	DGO0	Green
3	DBO5	Blue	20	GND	Ground
4	DBO4	Blue	21	DRO7	Red
5	GND	Ground	22	DRO6	Red
6	DBO3	Blue	23	DRO5	Red
7	DBO2	Blue	24	DRO4	Red
8	DBO1	Blue	25	GND	Ground
9	DBO0	Blue	26	DRO3	Red
10	GND	Ground	27	DRO2	Red
11	DGO7	Green	28	DRO1	Red
12	DGO6	Green	29	DRO0	Red
13	DGO5	Green	30	GND	Ground
14	DGO4	Green	31	VPP	Power Supply (+5 or +3.3V)
15	GND	Ground	32	VPP	Power Supply (+5 or +3.3V)
16	DGO3	Green	33	VPP	Power Supply (+5 or +3.3V)
17	DGO2	Green	34	VPP	Power Supply (+5 or +3.3V)

3.18.7. Panel Inverter Connector (1x11 PL176)

Pin	Symbol	Description	Pin	Symbol	Description
1,2,3	12V_INV	Inverter power supply	8	BKLON	
4	GND	Ground	9	GND	Ground
5	GND	Ground	10	PWMOUT	Brightness control
6,7	GND	Ground	11	GND	Ground

3.18.8. Keypad Card Connector (1x5 PL175)

Pin	Symbol	Pin	Symbol
1	Key1	6	Key3
2	Key2	7	Key4
3	GND	8	Key5
4	VCC5A (Analog +5V)	9	Key6
5	GND	10	Key7 or PWR_KEY

3.18.9. Optional Keypad Connector to UOC (1x2 PL 202)

Pin	Description
1	Data
2	Ground

3.18.10. LED & IR Receiver Connector (1x6 PL202)

Pin	Symbol	Description	Pin	Symbol	Description
1	ON/OFF or PWR_KEY		4	LED1	Led2 output
2	GND	Digital	5	IRRCVR	IR signal input
3	LED2	Led1 output	6	VCC5	Digital

3.18.11. Optional Rocker Sw. Connector (1x4 PL500)

Pin	Description
1,2	+12V External Power Supply In from JK500
3,4	Switched +12V

3.18.12. PROMJet Connector (2x25 PL101)

Pin	Symbol	Description	Pin	Symbol	Description
1,2	NC	Not connected	27-28	A[15-16]	Address
3	A[1]	Address	29-30	A[13-14]	Address
4	V3_3D	Digital 3.3V	31-32	A[11-12]	Address
5	GND		33-34	A[9-10]	Address
6	ROMOE	ROM output enable	35,36,37	NC	Not connected
7, 9, 11, 13	D[0-3]	Data	38	ROMWE	ROM write enable
8, 10, 12, 14	D[8-11]	Data	39	V3_3D	Digital 3.3V
15	V3_3D	Digital 3.3V	40,42	NC	Not connected
16, 18, 20, 22	D[4-7]	Data	41	A[19]	Address
17, 19, 21, 23	D[12-15]	Data	43-44	A[8],A[18]	Address
24	GND		45-46	A[6-7]	Address
25	V3_3D	Digital 3.3V	47-48	A[4-5]	Address
			49-50	A[2-3]	Address

3.18.13. Side HP Connector for Side-card Option (PL405)

Pin	Signal	Pin	Signal
1	Ground	4	HP-Left
2	HP-Right	5	Ground
3	Ground	6	HP switching signal HP_SW

3.18.14. Side AV Connector for Side-card Option (PL406)

Pin	Signal	Pin	Signal
1	Ground	4	Right Audio in
2	Left Audio in	5	Ground
3	Ground	6	CVBS in

3.18.15. Side SVHS Connector for Side-card Option (PL407)

Pin	Signal
1	Y-Luma
2	Ground
3	C-Chroma

4. SERVICE MENU SETTINGS

4.1. UOCIII Service Menu

- Turn on the TV.
- Press “Menu” (M) and “4” ”7” “2” “5” buttons of RC respectively. The following menu will displayed on the screen.

```
          GTV 3.2.1
000       EurAsia TVSub          05.01

00000000  00111100
01000000  01100100
11000101  01100100
00000000  01100100
```

- Enter register index number directly from RC or use P/CH + and P/CH – buttons in order to go any register setting.
- Press Volume + and Volume - buttons of RC in order to change the register value
- Press “TV” button from RC in order to turn the UOC service menu off.

4.1.1. UOCIII Service Menu Settings

- Check the following register values in the table from UOCIII Service Menu. Change them if they are not the same with the table below.

No :	Name:	Function:	Group:	Default:
0	EurAsia TVSub		GTV 3.2.1	05.01
1	Init TV	Sets the UOC default values and turns the tv to Stdby	GTV 3.2.1	0
2	ISP Mode	Sets the TV into ISP state.	GTV 3.2.1	0
3	DCXO	DCXO crystal alignment	Crystal alignment	70
4	DCXO Auto	Automatic DCXO frequency alignment. When it is set to 1; UOC automaticaly calculates DCXO values and writes it to item number 3.	Crystal alignment	0
5	Track. mode		Geometry	0
6	Rotation		Geometry	31
7	Hor. Shift		Geometry	32
8	HBL		Zoom	0
9	WBF		Zoom	4
10	WBR		Zoom	8
11	WSS	WSS (Wide Screen Siganling) enable	Zoom Options	1
12	Gld-SCART		Zoom Options	1
13	Col Fe	Color Saturation adjustment for RF input	Colour alignment	32
14	Col AV1	Color Saturation adjustment for Scart CVBS input	Colour alignment	32
15	Col AV1S		Colour alignment	32
16	Col AV2	Color Saturation adjustment for AV CVBS input	Colour alignment	32
17	Col AV2S	Color Saturation adjustment for for SVHS S-video input.	Colour alignment	32
18	BLOR		Colour alignment	32
19	BLOG		Colour alignment	32
20	RGB		Colour alignment	14
21	YSECAM	“Y delay” setting. (SECAM) (0-15)	Video	8
22	YNTSC	“Y delay” setting. (NTSC) (0-15)	Video	8
23	YPAL	“Y delay” setting. (PAL) (0-15)	Video	8
24	YAV1	“Y delay” setting. (SCART) (0-15)	Video	4
25	YAV2	“Y delay” setting. (FAV) (0-15)	Video	4

No：	Name:	Function:	Group:	Default:
26	YSVHS1	“Y delay” setting. (0-15)	Video	4
27	YSVHS2	“Y delay” setting. (S-Video) (0-15)	Video	4
28	ACL		Bit Control	0
29	MUS		Bit Control	0
30	PWL		Bit Control	8
31	CB		Bit Control	0
32	BPS		Bit Control	0
33	FCO		Bit Control	0
34	PeakFreqPAL443		Video	1
35	PeakFreqPALM		Video	1
36	PeakFreqPALN		Video	1
37	PeakFreqNTSC443		Video	1
38	PeakFreqNTSCM		Video	1
39	PeakFreqSECAM		Video	1
40	PeakFreqAV		Video	1
41	Blackstretch		Video options	1
42	Bluestretch		Video options	0
43	Whitestretch		Video options	0
44	Transfer Rato		Video Option	1
45	PeakRatioOvShot		Video	2
46	Tint NTSC		Video	31
47	OSO		Bit Control	0
48	FSL		Bit Control	0
49	HP2		Bit Control	0
50	SoftClipLevel		Bit Control	0
51	OP AUDIO CONFIG		Audio options	2
52	OP BILING		Audio options	1
53	OP HP		Audio options	1
54	OP EQUAL		Audio options	1
55	OP DOLBY		Audio options	0
56	OP TRUSUR		Audio options	0
57	OP DUB DBE		Audio options	0
58	OP BBE		Audio options	0
59	AVL-LEV	AVL level setting	Audio	1
60	AVL-WGT	AVL weight setting	Audio	1
61	AVL-MOD	AVL response time setting	Audio	3
62	AVLE	AVL enable/disable	Audio	1
63	LOUD-NA		Audio	5
64	LOUD-CH		Audio	1
65	BBE-CONT		Audio	7
66	BBE-PROC		Audio	7
67	OP CLIP		Audio	0
68	DEC-LEV	FM German Str. Prescale setting	Audio	23
69	MONO-LEV	FM Mono Prescale setting	Audio	23
70	NIC-LEV	Nicam Str. Prescale setting	Audio	17
71	ADC-AM-L	AM Mono Prescale setting	Audio	21
72	ADC-AV-L	Scart/Line in Prescale setting	Audio	18
73	BGSCAL DEC		Audio	0
74	BGSCAL MONO		Audio	0

No：	Name:	Function:	Group:	Default:
75	BGSCAL NIC		Audio	0
76	BGSCAL SAP		Audio	0
77	MSCAL DEC		Audio	0
78	MSCAL MONO		Audio	0
79	MSCAL NIC		Audio	0
80	MSCAL SAP		Audio	0
81	LSCAL DEC		Audio	0
82	LSCAL MONO		Audio	0
83	LSCAL NIC		Audio	0
84	LSCAL SAP		Audio	0
85	E2D		Audio	0
86	FFI		Audio	0
87	CMUTE		Audio	1
88	PA-BA-VO		Audio Preset	31
89	PA-TR-VO		Audio Preset	15
90	PA-LM-VO		Audio Preset	1
91	PA-ST-VO		Audio Preset	5
92	PA-LO-VO		Audio Preset	0
93	PA-B1-VO		Audio Preset	21
94	PA-B2-VO		Audio Preset	50
95	PA-B3-VO		Audio Preset	55
96	PA-B4-VO		Audio Preset	45
97	PA-B5-VO		Audio Preset	34
98	PA-BA-MU		Audio Preset	34
99	PA-TR-MU		Audio Preset	39
100	PA-LM-MU		Audio Preset	1
101	PA-ST-MU		Audio Preset	5
102	PA-LO-MU		Audio Preset	1
103	PA-B1-MU		Audio Preset	52
104	PA-B2-MU		Audio Preset	47
105	PA-B3-MU		Audio Preset	29
106	PA-B4-MU		Audio Preset	29
107	PA-B5-MU		Audio Preset	45
108	PA-BA-TH		Audio Preset	36
109	PA-TR-TH		Audio Preset	34
110	PA-LM-TH		Audio Preset	1
111	PA-ST-TH		Audio Preset	5
112	PA-LO-TH		Audio Preset	0
113	PA-B1-TH		Audio Preset	47
114	PA-B2-TH		Audio Preset	45
115	PA-B3-TH		Audio Preset	42
116	PA-B4-TH		Audio Preset	45
117	PA-B5-TH		Audio Preset	42
118	AGC Speed	AGC speed setting	Tuning	1
119	AGC Take over	AGC setting	Tuning	27
120	OIF	IF Demodulator OffSet	Tuning	32
121	IF	IF Frequency	Tuning	2
122	SVO		Bit Control	0
123	GD		Bit Control	1

No:	Name:	Function:	Group:	Default:
124	BPB		Source Switching	0
125	BPB2		Source Switching	0
126	RGB-IN		Source Switching	1
127	DVD1-IN		Source Switching	0
128	AV2-IN		Source Switching	1
129	DVD2-IN		Source Switching	0
130	AV1S-IN		Source Switching	0
131	AV1D-IN		Source Switching	0
132	AV2S-IN		Source Switching	1
133	CBVS-OUT		Source Switching	1
134	INCL-AV		Source Switching	0
135	TXT-ON		Teletext options	1
136	TXT-SPLIT		Teletext options	1
137	TXT-H-POS		Teletext options	11
138	TIM-REM		Timer options	1
139	TIM-SLP		Timer options	1
140	TIM-SW		Timer options	1
141	TIM-OFF		Timer options	1
142	TIM-SKP		Timer options	1
143	TIM-RT		Timer options	1
144	FM Radio		FM Radio options	1
145	PWR-SAVING		Power options	1
146	PWR-PERF		Power options	3
147	PWR-REST		Power options	0
148	PWR-ONKEY		Power options	1
149	Factory Mode		GTV 3.2.1	0
150	CombFil	Combfilter enable/disable	Video options	1
151	BlueBlackNoMute		Video options	0
152	ATS		Installation opt.	1
153	EVG		Bit Control	0
154	DFL		Bit Control	0
155	XDT		Bit Control	0
156	AKB		Bit Control	1
157	OSVE		Bit Control	0
158	CL		Colour alignment	10
159	LCD-BRT	UOC Brightness	Sub System	36
160	LCD-CON	UOC Contrast	Sub System	32
161	LCD-CON-FE	RF frontend contrast adjust.	Sub System	30
162	LCD-CON-AV1	Scart CVBS contrast adjust.	Sub System	32
163	LCD-CON-AV1S		Sub System	32
164	LCD-CON-AV2	AV CVBS contrast adjust.	Sub System	32
165	LCD-CON-AV2S	S-Video input contrast adjust.	Sub System	32
166	RBL		Sub System	0
167	EGL		Sub System	0
168	LPG		Sub System	1
169	PGR	UOC Red Contrast	Sub System	32
170	PGG-CVBS	UOC Green Contrast for CVBS input	Sub System	32
171	PGG-RGB	UOC Green Contrast for RGB input	Sub System	34
172	PGB	UOC Blue Contrast	Sub System	32

4.1.2. Tuner AGC Alignment

In this part, tuner AGC alignment procedure is described.
A TV pattern generator with RF output and volt-meter are needed for this alignment.

Test Set-up
"NICAM Stereo" and 60 dB PAL B/G RF signal from pattern generator will be applied. Frequency must be set to 224.25 MHz.

- Turn on the TV and measure the AGC voltage from Tuner Pin1 without plugging in any RF input (Around 4.12V).
- Apply "NICAM Stereo" and 60 dB(1 mV) PAL B/G RF signal to the tuner input.
- Enter UOC service menu (as described above), and go to "AGC Take over" setting by pressing "1" "1" "8".
- Measure AGC voltage from Tuner Pin1. By pressing Volume +/-; adjust AGC voltage so that the measured value at this step should be 0,5V less than the value measured at first step (Around 3.5V).

4.1.3. DCXO Alignment

If this alignment has not properly been done, some front end RF problems can be observed such as Nicam stereo / mono sound switching, low RF reception and color separation performance.

Test Set-up
This alignment will be performed just after Tuner AGC Alignment. Apply "NICAM Stereo" and 60 dB PAL B/G RF signal from pattern generator. Frequency must be set to 224.25 MHz.

- Turn on the TV.
- Enter UOC service menu (as described above), and go to "DCXO Auto" setting.
- Set "DCXO Auto" value to "1" by pressing "Volume +".
- TV will automatically align the DCXO (Digital Controlled Xtal Oscillator) value.
- Then TV automatically re-sets "DCXO Auto" value to "0". This indicates that DCXO Alignment successfully completed.

4.2. PW1306 Service Menu

- In order to work with PW service menu:
- Press "Menu" (M) and "4" "7" "2" "6" buttons of RC respectively.
- Make the desired settings.
- Press "Menu" (M) from RC to turn off the PW Service menu
- The menu has the following structure:

Service Menu

Service Submenu1		Service Submenu2		Service Submenu3	
Dclock Polarity	Falling	Init NVM		Country	***
UOC Hposition	*	Initial APS	off	Language	***
ADC_Calibration				Pannel Type	LG17WXGA_V3
UOC_Calibration				Menu Background	Opaque
**				Remote Control	***

* This value indicetes the horisontal positioning of the picture.
** In this row "Software version and date is mentioned"
*** These will be changed according to the DI.

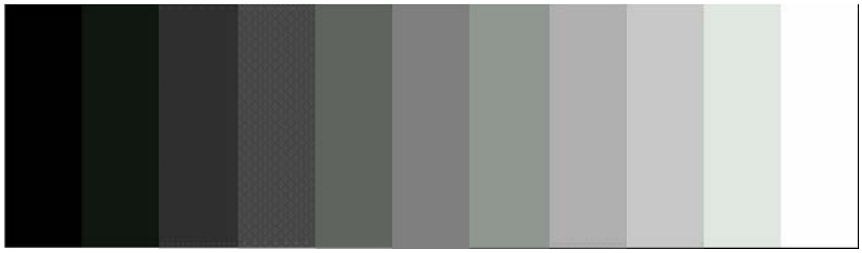
- It is possible to move by using “UP”, “DOWN”, “LEFT” and “RIGHT” RC buttons in this menu structure.

4.2.1. UOC Horizontal Position

- Press “DOWN” RC button at “Service Submenu 1” to highlight “UOC Hposition”
- Set the proper value to fit the applied pattern to screen by using “LEFT” and ”RIGHT” buttons.

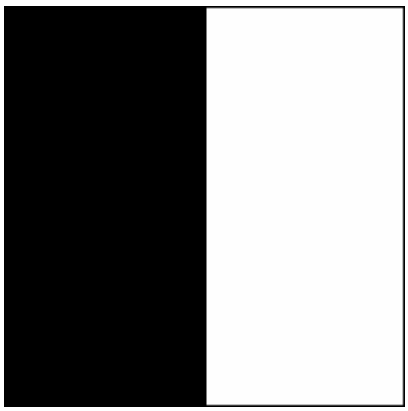
4.2.2. UOC Calibration

- Apply 11 Vertical bar Grey-scale pattern with black on the left and white on the right side of the picture(as seen below) from CVBS input.
- Press RC “AV” button, and switch to CVBS input and observe the pattern applied.
- Enter to PW1306 service menu.
- Press RC “DOWN” button at “Service Submenu 1” and highlight “UOC Calibration”.
- Press RC “RIGHT” button to start calibration.



4.2.3. PW1306 PC Input ADC Calibration

- Connect your TV with your PC and press RC “PC” button and observe the image.
- Press “M” to display Menu and select “Options” by using right button of RC.
- Press “Down” button of the RC and activate “auto adjustment”.
- Press right button of the RC to perform “auto adjustment” and press “M” to exit from Menu.
- Apply black on the left, white on the right(as seen below) XGA@60Hz (1024x768) pattern from PC.
- Enter PW1306 service menu as described above.
- Press RC “DOWN” button at “Service Submenu 1” and highlight “ADC Calibration”.
- Press RC “RIGHT” button to start calibration.



4.2.4. Init NVM

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “DOWN” button and highlight “”Init NVM”
- Press RC “RIGHT” button to set TV to initial settings. Next time TV is turned on, default settings will be loaded to TV.

4.2.5. Initial APS

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “DOWN” button and highlight “”Initial APS”

Press RC “RIGHT” and “LEFT” buttons to set Initial APS to “on” or “off”.(When Initial APS is set to “on” TV will display “Initial APS” menu at first time it is turned on)

4.2.6. Country

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “RIGHT” button at “Service Submenu 2” and switch to “Service Submenu 3”
- Press RC “DOWN” button and highlight ”Country”
- Press RC “RIGHT” and “LEFT” buttons to set the desired country option.

4.2.7. Language

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “RIGHT” button at “Service Submenu 2” and switch to “Service Submenu 3”
- Press RC “DOWN” button and highlight ”Language”
- Press RC “RIGHT” and “LEFT” buttons to set the desired language option.

4.2.8. Menu Background

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “RIGHT” button at “Service Submenu 2” and switch to “Service Submenu 3”
- Press RC “DOWN” button and highlight “Menu Background”.
- Press RC “RIGHT” and “LEFT” buttons to set menu background to “opaque” or translucent.

4.2.9. Remote Control

- Press RC “RIGHT” button at “Service Submenu 1” and switch to “Service Submenu 2”
- Press RC “RIGHT” button at “Service Submenu 2” and switch to “Service Submenu 3”
- Press RC “DOWN” button and highlight ”Remote Control”
- Press RC “RIGHT” and “LEFT” buttons to set the desired remote control option.

4.3. Panel Type Change Shortcut

As 17MB18 software supports from 14” to 20” panel types, it is possible not to see anything on the screen after Init NVM as the default panel type is 15” in the software. That s why, a hidden menu is needed to change supported panel from a hidden menu which is not shown on the screen.

In order to work with PW panel type selection shortcut service menu:

- Press “Menu” (M) and “4” ”7” “2” “7” buttons of RC respectively. (Caution! No visual menu will appear on the screen)
- Press individual panel type selection digit to select the panel (see below table).
- Turn off the TV from RC.

When the TV turns on again, it will come with new panel settings.

Hidden Menu Panel types:

Panel type selection digit	Panel
0	15” Samsung
1	20” CMO
2	17” LG

5. PRODUCTION SETTINGS AND FACTORY DEFAULTS

5.1. Production Schedule

- UOCIII Programming before test Jig

Settings that will be performed on the Test Jig.

- Tuner AGC Alignement (Section 4.1.2).
- DCXO Alignement (Section 4.1.3)
- UOC Calibration (Section 4.2.2)
- PW1306 PC Input ADC Calibration (Section 4.2.3)

Settings that will be performed on the Production Band
DDC programming.

5.2. EEPROM Settings

5.2.1. Creating Master EEPROM

- Load the new SW version to the TV.
- Place empty EEPROM to IC101 position of the mainboard.
- Turn on the TV.SW will automatically assign the initial values to the EEPROM.
- Adjust the settings of Service Menu and User Menu.
- This EEPROM can be used as Master EEPROM.

5.2.2. Creating Mass Production EEPROM

- The Master EEPROM prepared like above is copied and multiplied to use in mass production.
- The copy EEPROM is placed on IC 101 of 17MB18. (When TV is turned on the software will realise that EEPROM is not empty, so SW will not change the values in the EEPROM.)

5.3. TV Menu

5.3.1. Picture Menu

Picture	
brightness	*
contrast	*
filter	sharp
sharpness	51
color	64
Tint	*xx*

* Brightness and contrast values will be left unchanged after the UOC Calibration.

xx Tint value is determined automatically by software and is active in only NTSC channels. So there is no need to adjust any value in this section.

5.3.2. Audio Menu

Audio		
volume	29	

balance	49			
AVL	On			
extended audio features				
Feature		headphone		equalizer
effect	normal	volume	10	**
sound style	user	balance	49	

** Will be left unchanged as they are adjusted in the EEPROM.

5.3.3. Window Menu

Window	
image size	auto
white tone	normal
dynamic skin tone	off

5.3.4. Options Menu

Options	
menu background	opaque
Language	***
room lighting	bright
sleep time	0
child lock	off

*** Will be changed according to the DI.

5.3.5. Settings Menu

Installation				
	Channel Setup		APS	
	program number	****	country	***
	program name	****	aps	
	manual search	****		
	standard	Auto		
	store	****		
	frequency	****		
	fine tuning	****		
	program skip	Off		
teletext language	Europe			
teletext region	West			

**** Will change according to the user and the country it is used.

5.4. PC Mode Menu

5.4.1. Picture Menu

Picture	
brightness	*
contrast	*
filter	Sharp
phase	**
frequency	50

* Brightness and contrast values will be left unchanged after the UOC Calibration

** Phase value is automatically set by the software. There is no need to adjust any value in this section.

5.4.2. Audio Menü

Audio					
volume	29				
balance	49				
AVL	on				
extended audio features					
	Feature		headphone		Equilizer
	Effect	normal	volume	10	***
	sound style	user	balance	49	

*** Will be left unchanged as they are adjusted in the EEPROM.

5.4.3. Window Menu

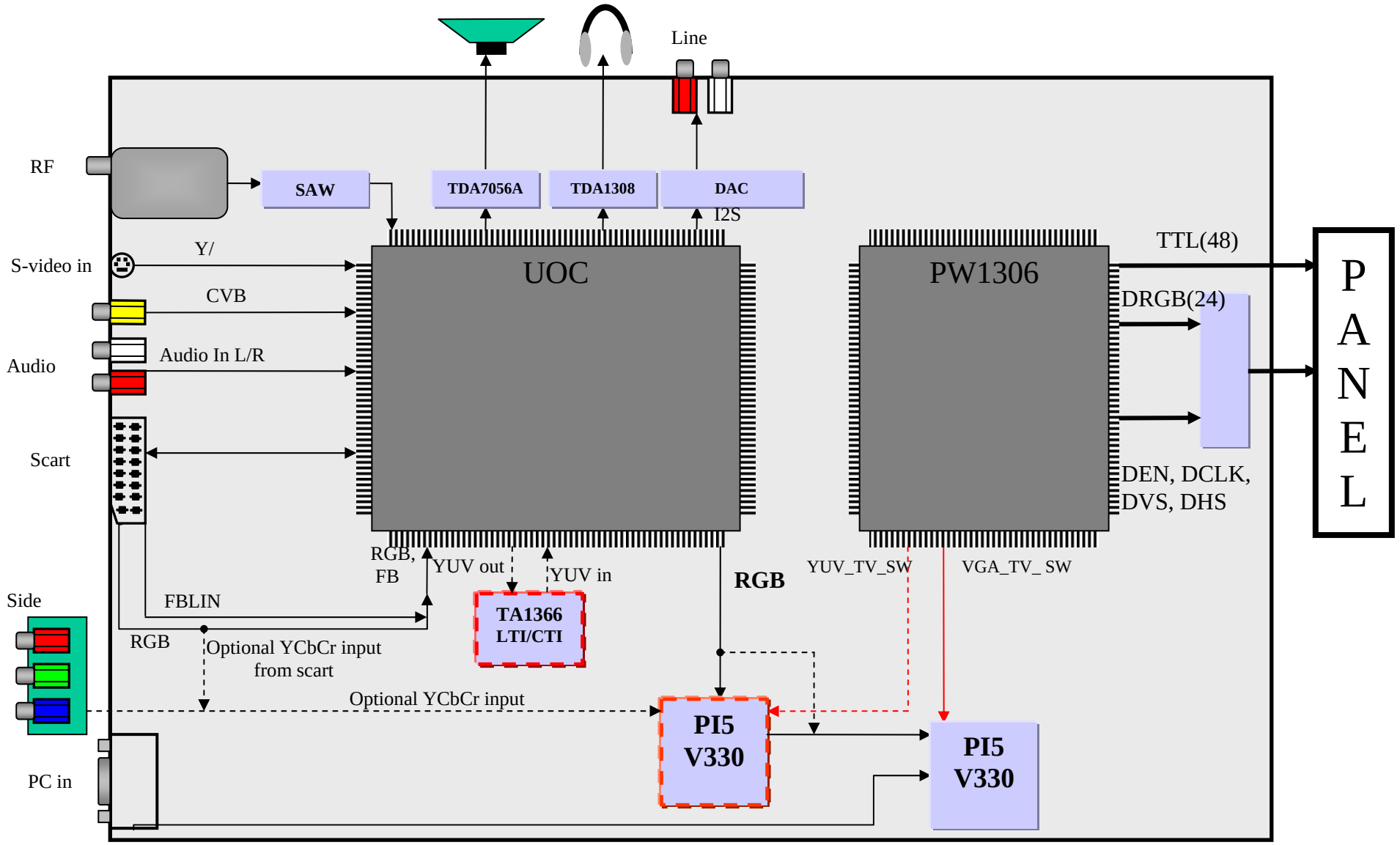
Window	
H-Position	50
V-Position	50

5.4.4. Options Menü

Options	
menu background	opaque
Language	****
room lighting	normal
auto adjustment	
child lock	off

**** Will be changed according to the DI.

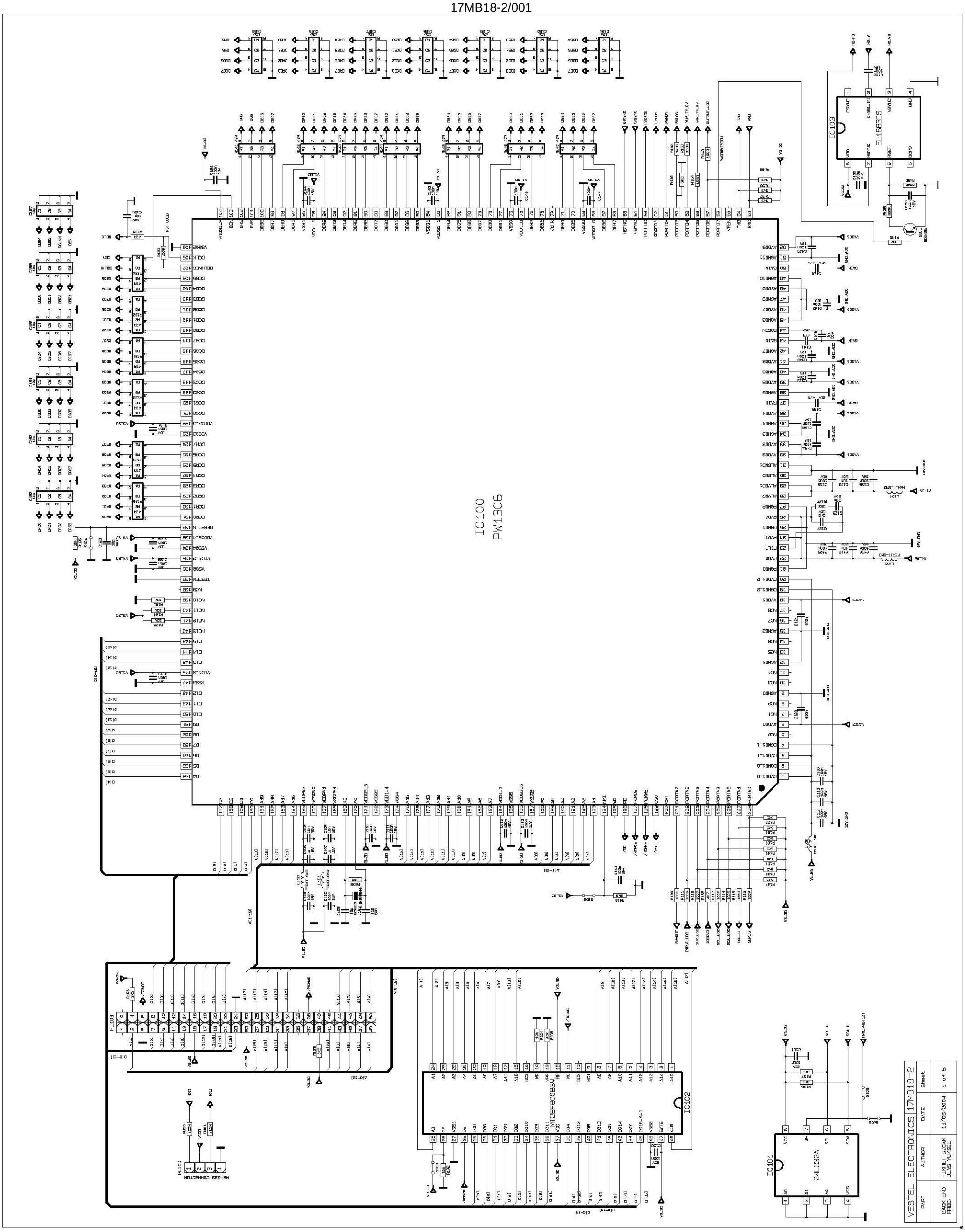
6. BLOCK DIAGRAM

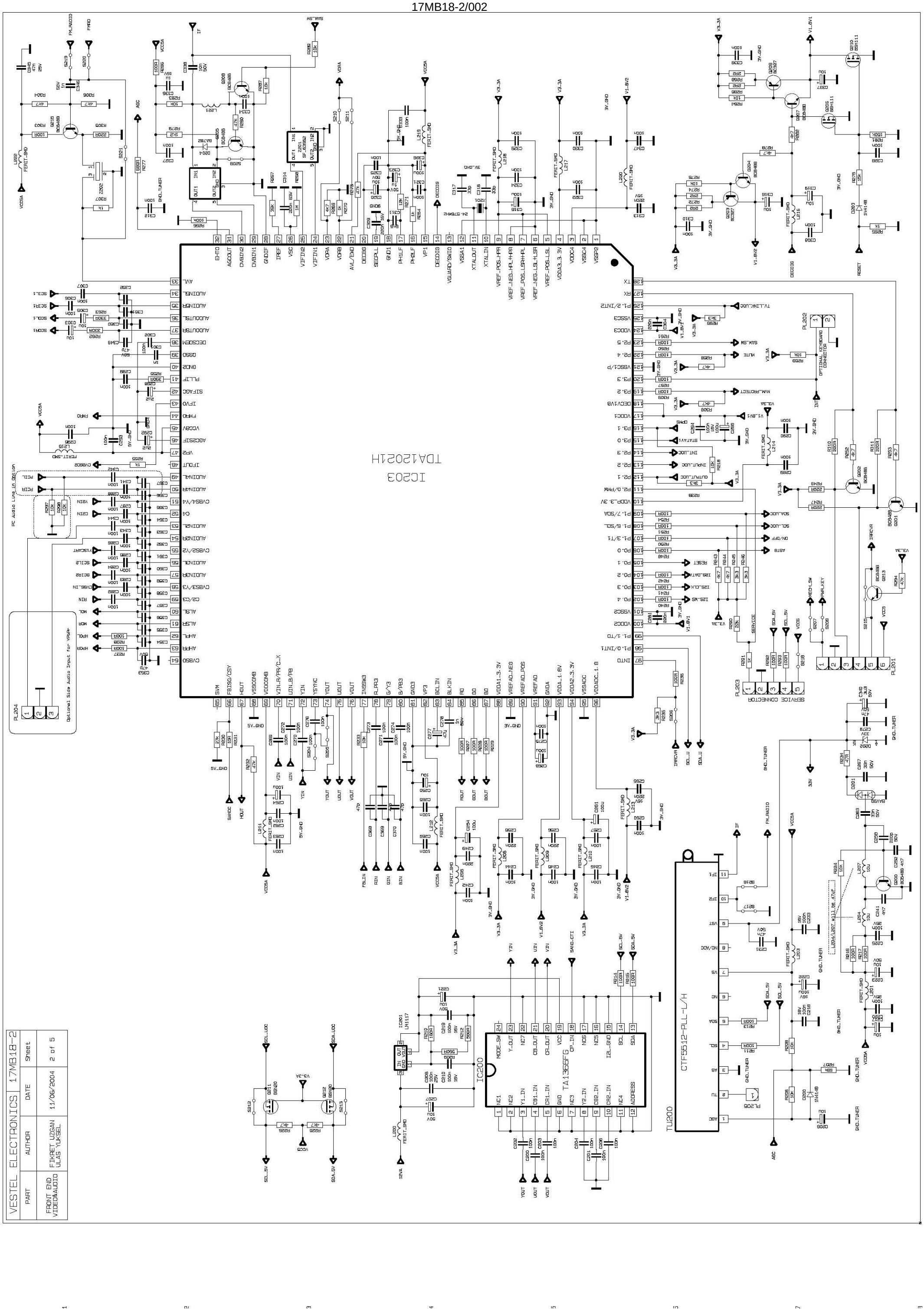


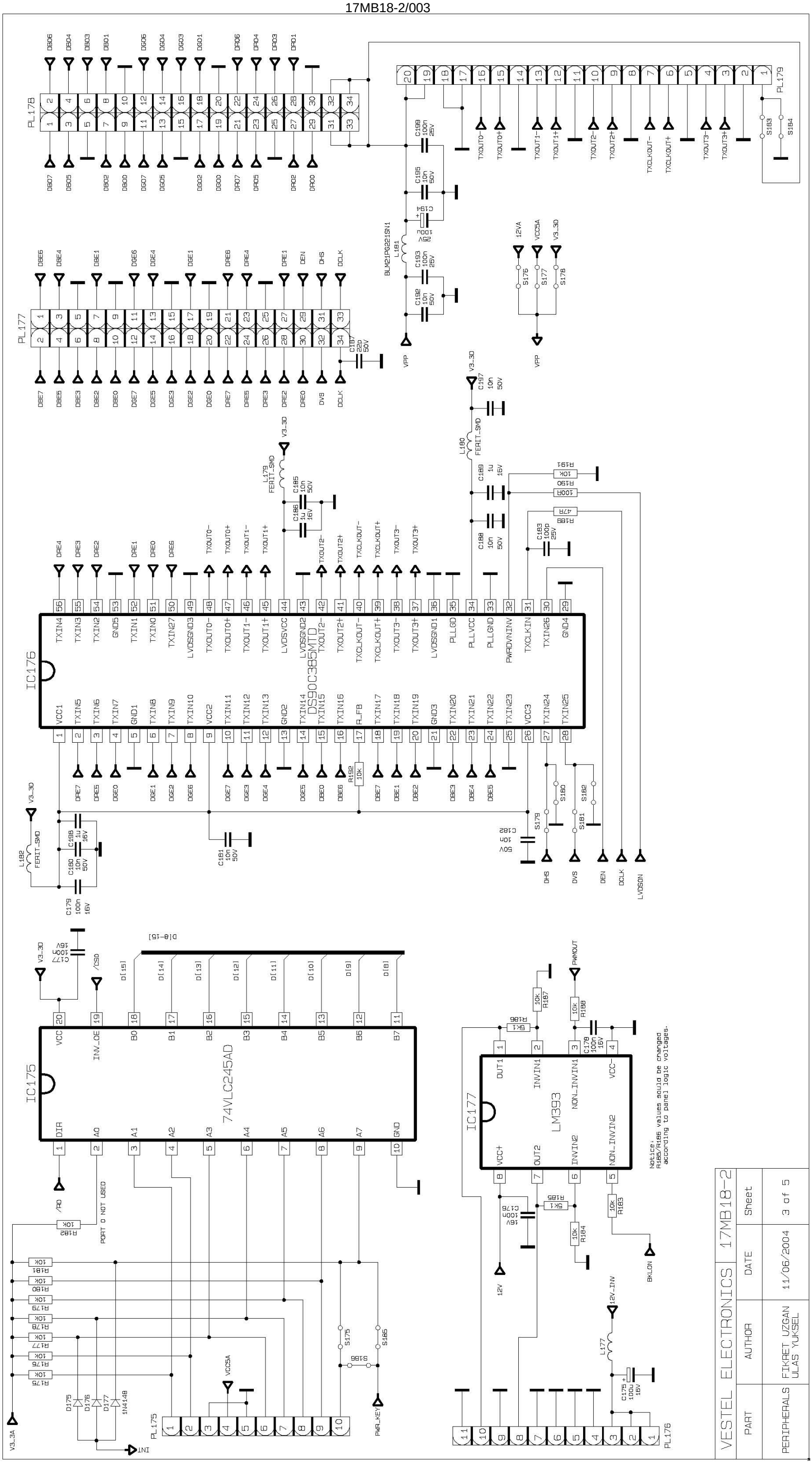
7. CIRCUIT DIAGRAMS

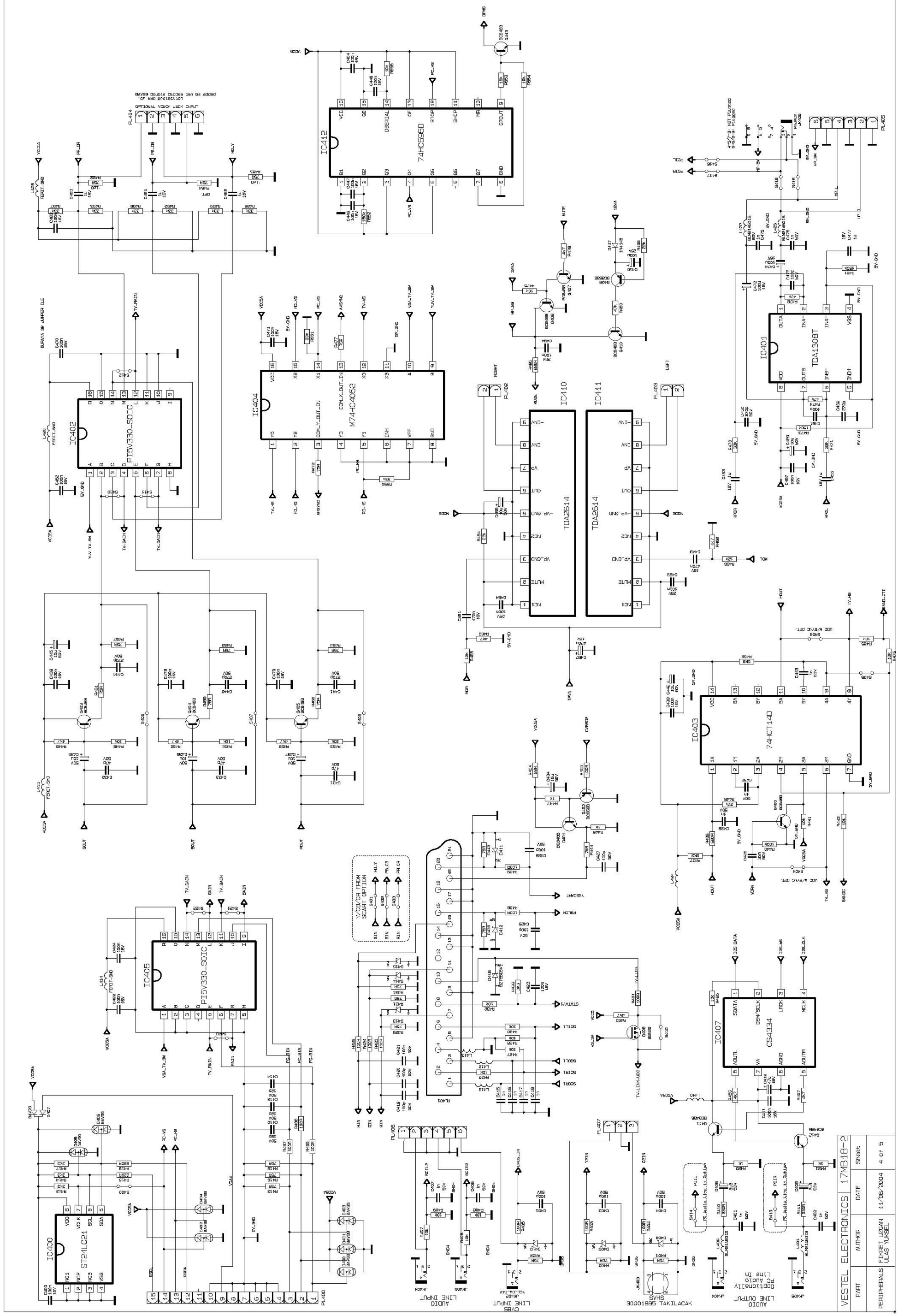
7.1. 17MB18 Main Board Schematics

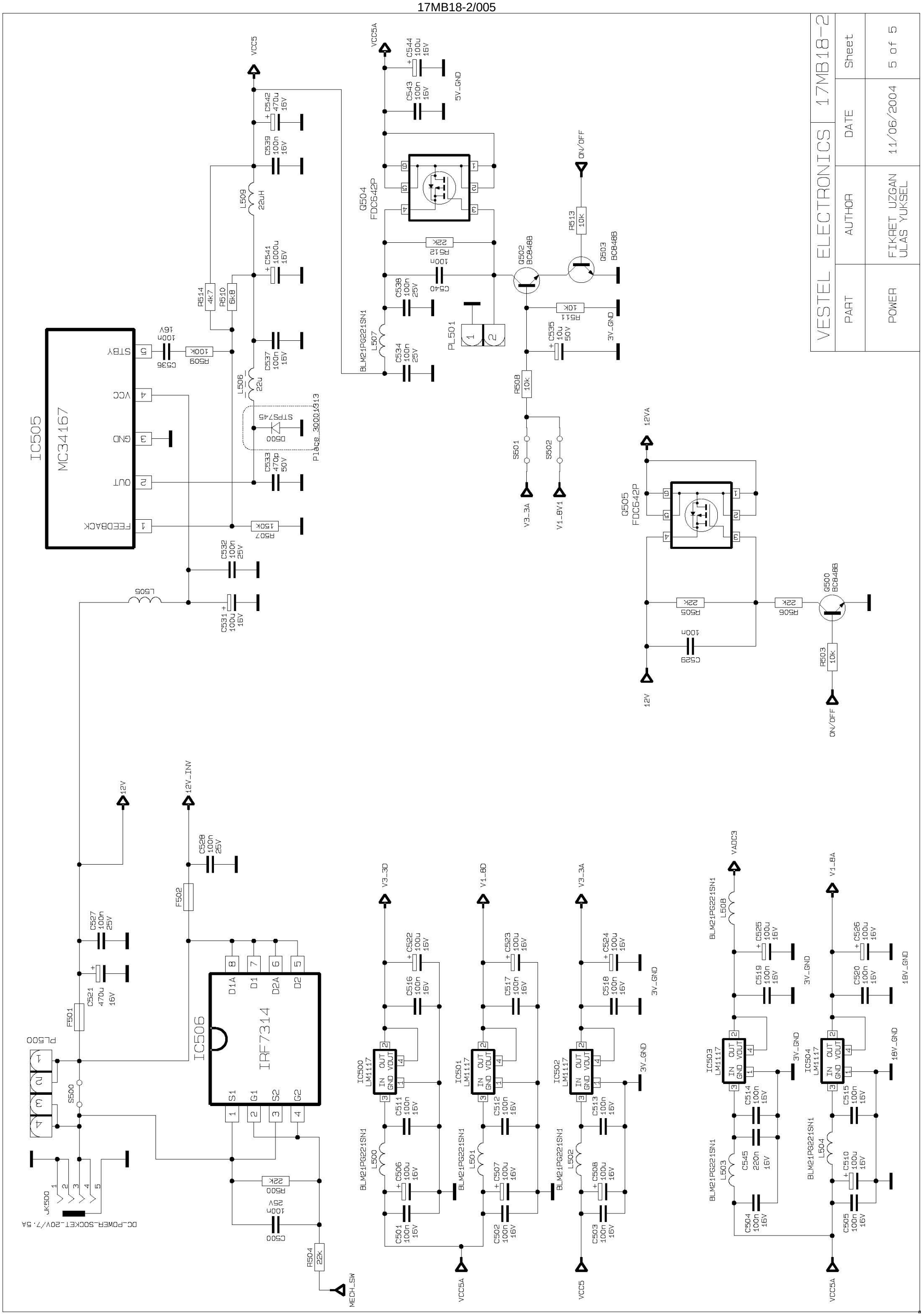
17MB18-2/001



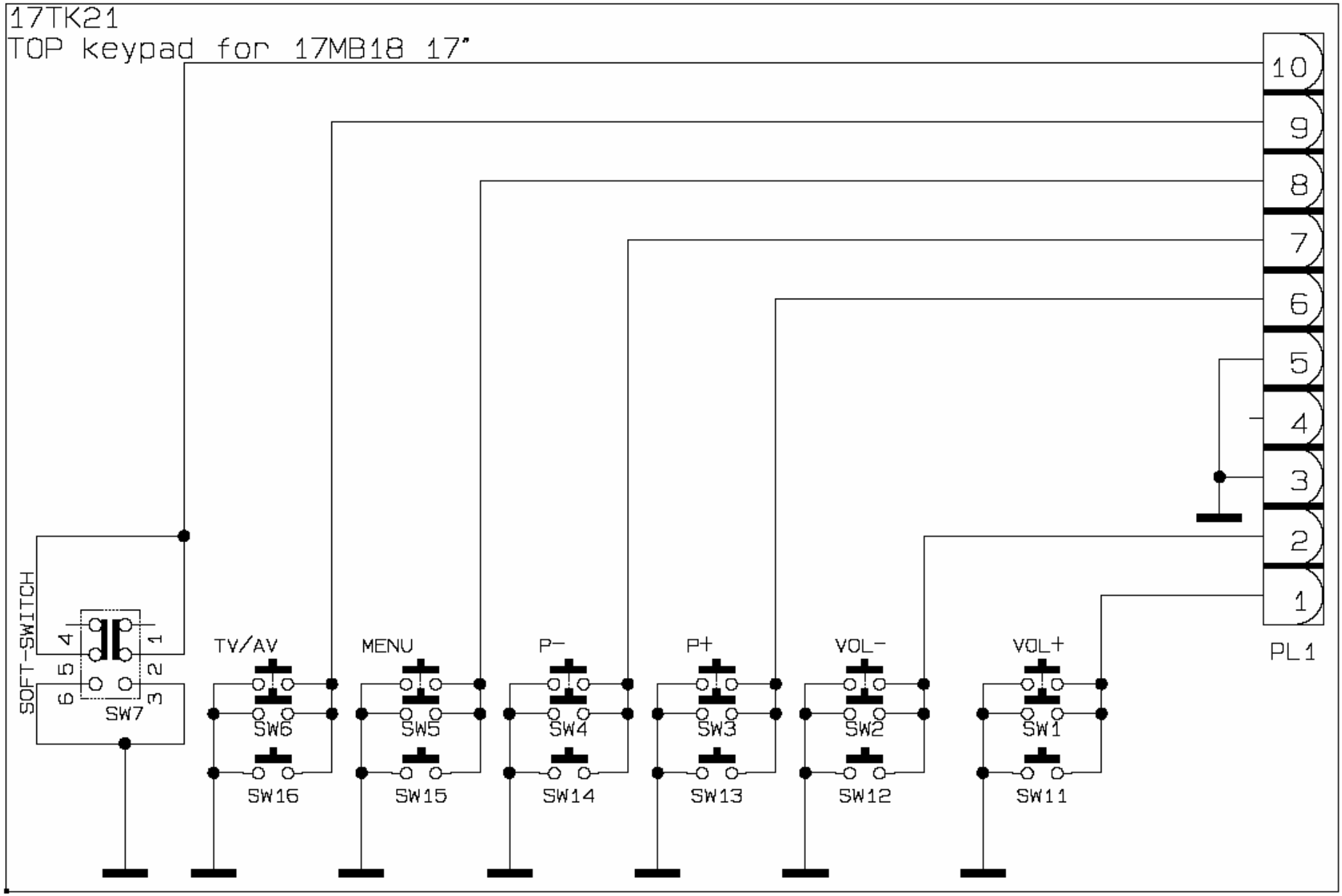

IC203
TDA12021H
IC200
TA1366F6
TU200
CTF5512-PLL-L/H
VESTEL ELECTRONICS | 17MB18-2
PART: FRONT END VIDEO&AUDIO
AUTHOR: FIKRET UZGAN ULAS YUKSEL
DATE: 11/06/2004
Sheet: 2 of 5


PL178
PL179
PL177
IC176
DS90C385MTD
IC175
74VLC245AD
IC177
LM393
PL175
PL176
L181
BLM21PG221SN1
L182
L179
L180
L177
FERIT_SMD
VESTEL ELECTRONICS
17MB18-2
PART
PERIPHERALS
AUTHOR
FIKRET UZGAN
ULAS YUKSEL
DATE
11/06/2004
Sheet
3 of 5
Notice:
R185/R186 values sould be changed
according to panel logic voltages.


IC412
74HC595D
IC404
M74HC4052
IC410
IC411
TDA2614
IC401
TDA1308T
IC402
PI5V330-SOIC
IC403
74HCT14D
IC405
IC407
CS4334
IC400
ST24LC21
VESTEL ELECTRONICS
17MB18-2
PART
AUTHOR
DATE
Sheet
PERIPHERALS
FIKRET UZGAN
ULAS YUKSEL
11/06/2004
4 of 5

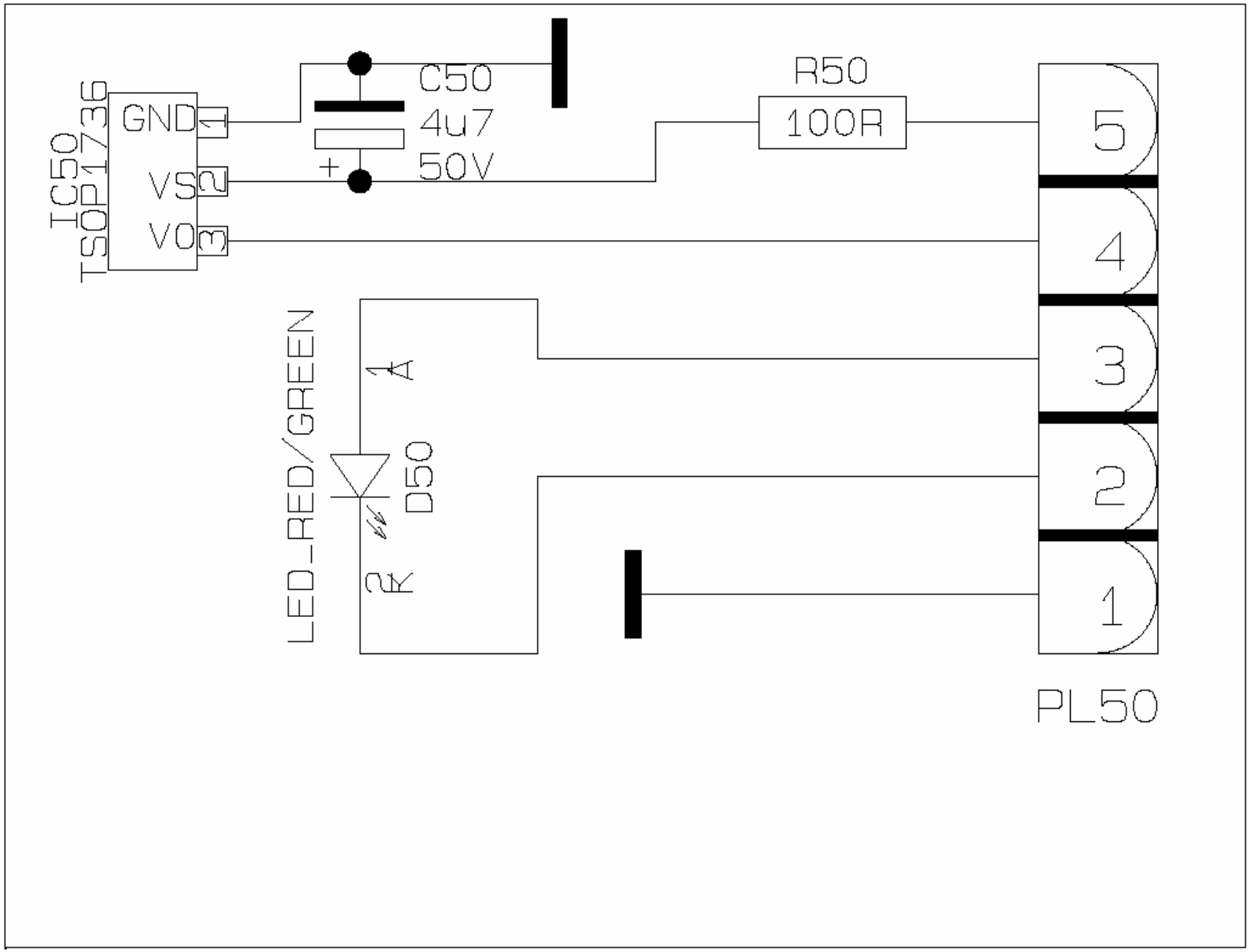

VESTEL ELECTRONICS
17MB18-2
PART
POWER
AUTHOR
FIKRET UZGAN
ULAS YUKSEL
DATE
11/06/2004
Sheet
5 of 5
IC505
MC34167
STBY
VCC
GND
OUT
FEEDBACK
IC506
IRF7314
D1A
D1
D2A
D2
S1
G1
S2
G2
Q504
FDC642P
Q505
FDC642P
Q502
BC848B
Q503
BC848B
Q500
BC848B
PL501
PL500
JK500
DC_POWER_SOCKET_20V/7.5A
S500
S501
S502
D500
STPS745
Place_3000813
L509
22uH
L506
22u
L507
BLM21PG221SN1
L505
L500
L501
L502
L503
L504
L508
F501
F502
IC500
IC501
IC502
IC503
IC504
LM1117
IN
OUT
GND
VOUT
ON/OFF
MECH_SW
12V
12VA
12V_INV
5V_GND
3V_GND
1V8_GND
VCC5
VCC5A
V3_3D
V1_8D
V3_3A
V1_8A
V3_3A
V1_8V1
VADC3
R514 4k7
R510 6k8
R509 100K
R507 150K
R508 10K
R511 10K
R513 10K
R503 10K
R504 22k
R500 22K
R505 22K
R506 22K
R512 22K
C536 100n 16V
C537 100n 16V
C538 100n 25V
C534 100n 25V
C540 100n
C535 10u 50V
C539 100n 16V
C542 470u 16V
C541 1000u 16V
C544 100u 16V
C543 100n 16V
C533 470p 50V
C532 100n 25V
C531 100u 16V
C528 100n 25V
C527 100n 25V
C521 470u 16V
C500 100n 25V
C529 100n
C501 100n 16V
C502 100n 16V
C503 100n 16V
C504 100n 16V
C505 100n 16V
C506 100u 16V
C507 100u 16V
C508 100u 16V
C510 100u 16V
C511 100n 16V
C512 100n 16V
C513 100n 16V
C514 100n 16V
C515 100n 16V
C516 100n 16V
C517 100n 16V
C518 100n 16V
C519 100n 16V
C520 100n 16V
C522 100u 16V
C523 100u 16V
C524 100u 16V
C525 100u 16V
C526 100u 16V
C545 220n 16V

7.2. Keypad Schematics

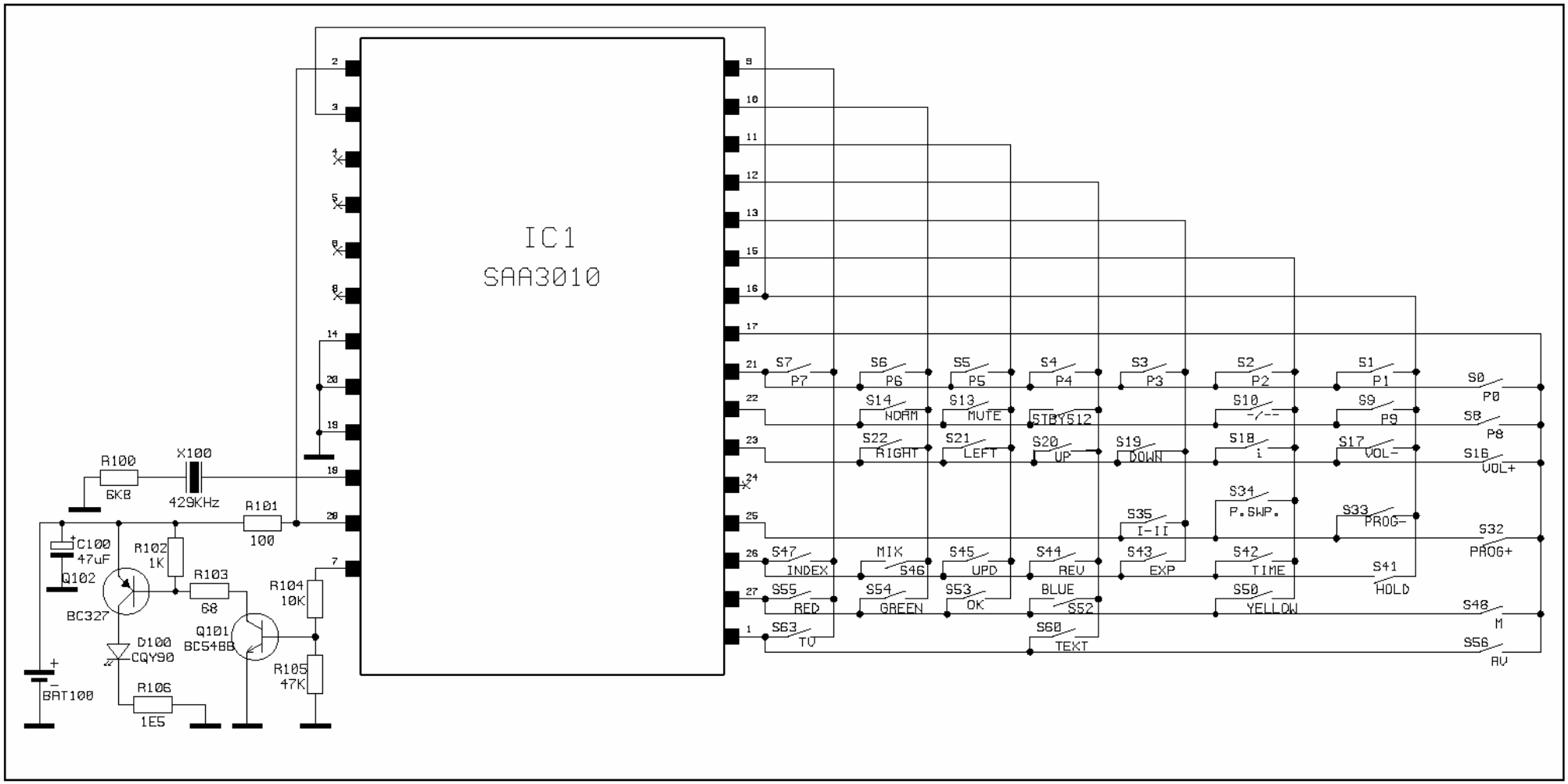


17TKXX

7.3. IR&LED Board Schematics



7.4. Remote Controller Schematics



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